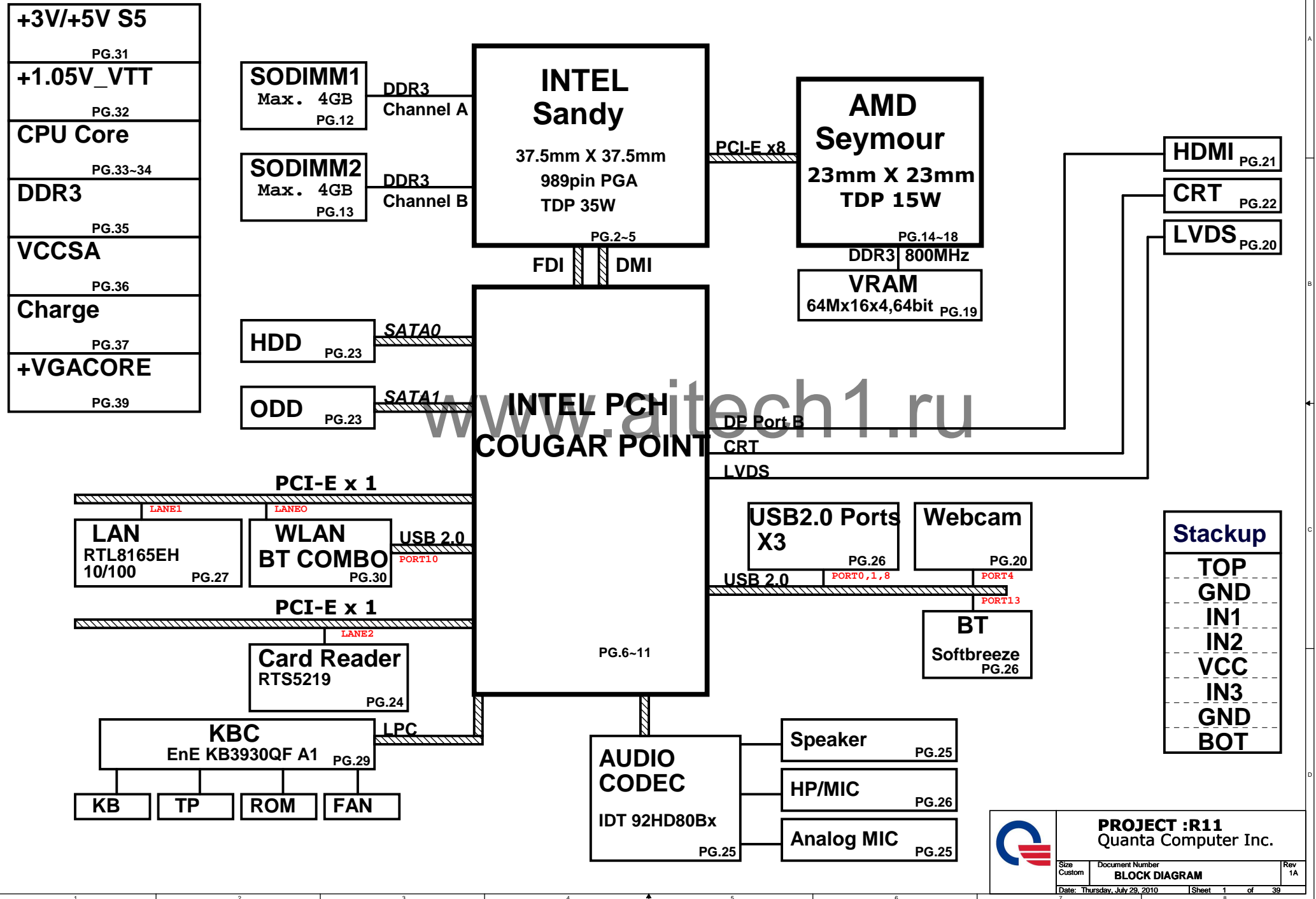
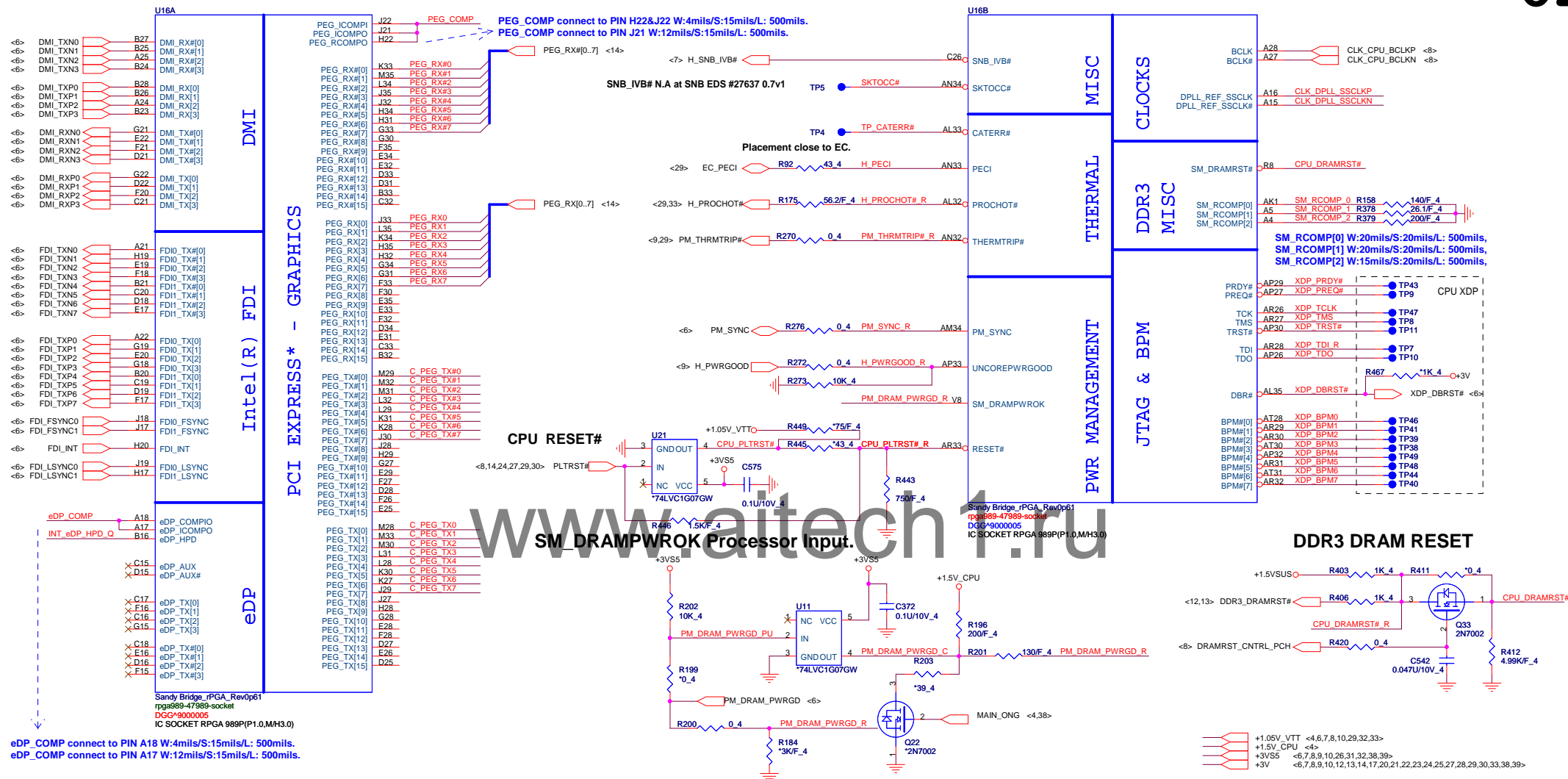
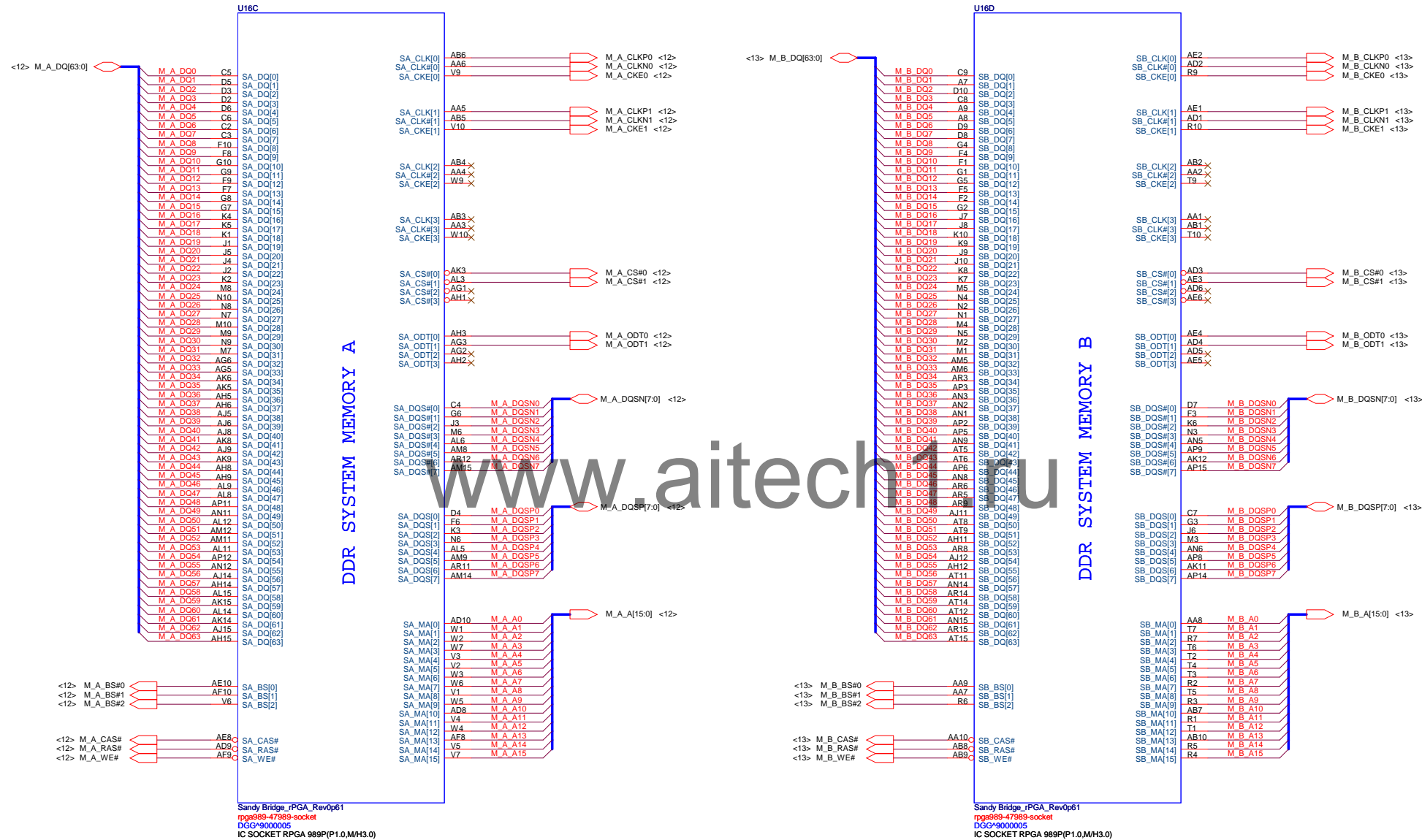


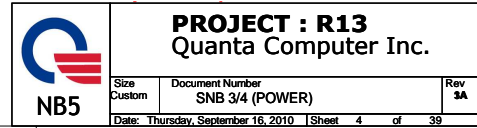
R11 INTEL UMA/DISCRETE SYSTEM DIAGRAM 01

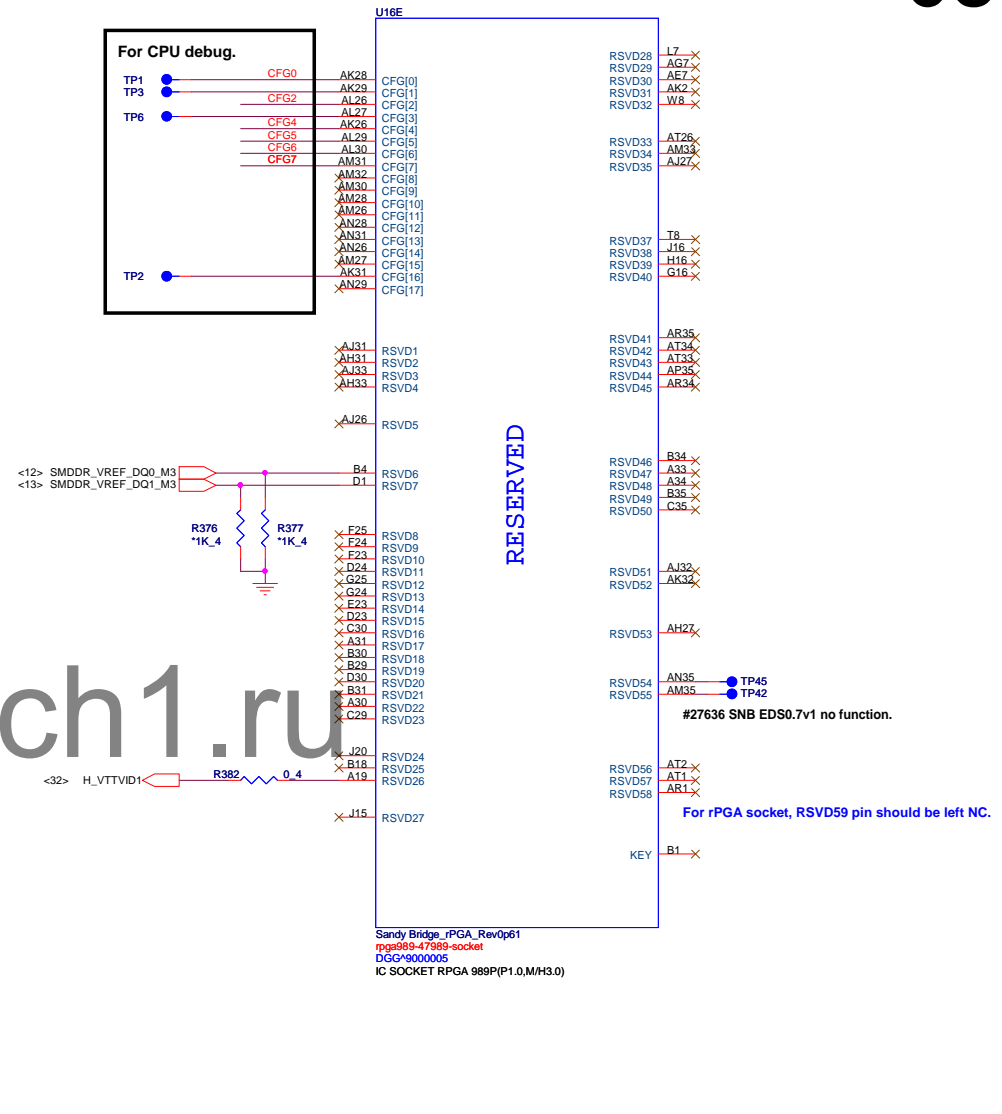




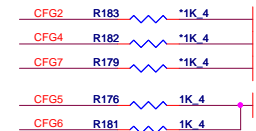
Sandy Bridge Processor (DDR3)

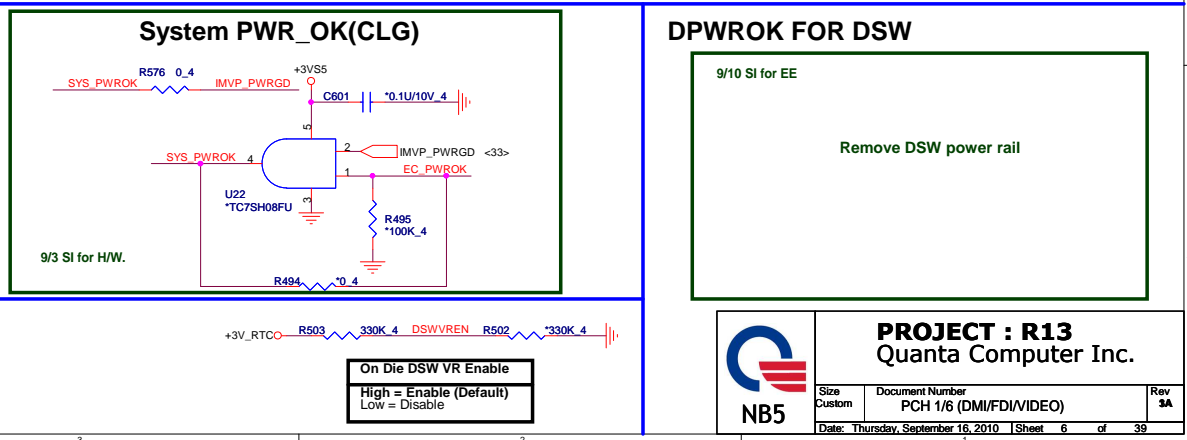
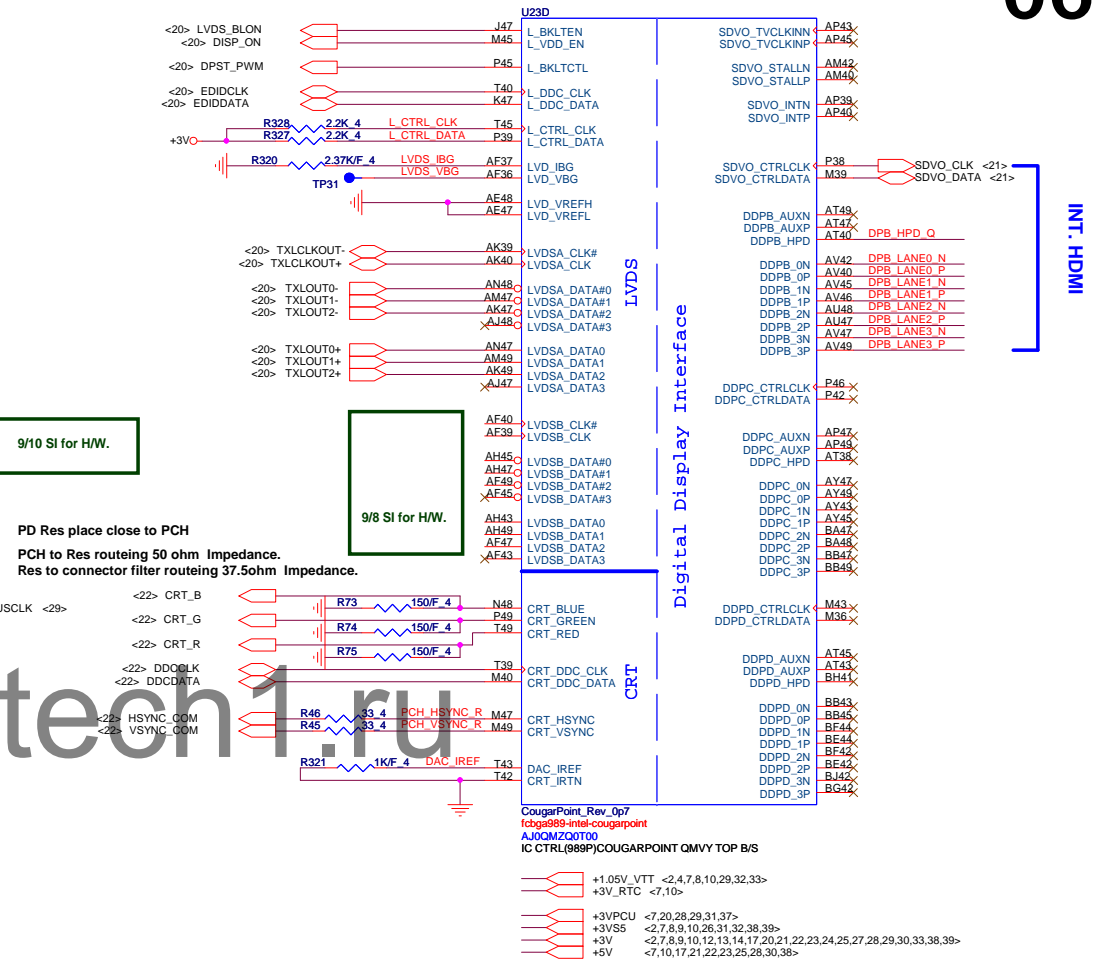




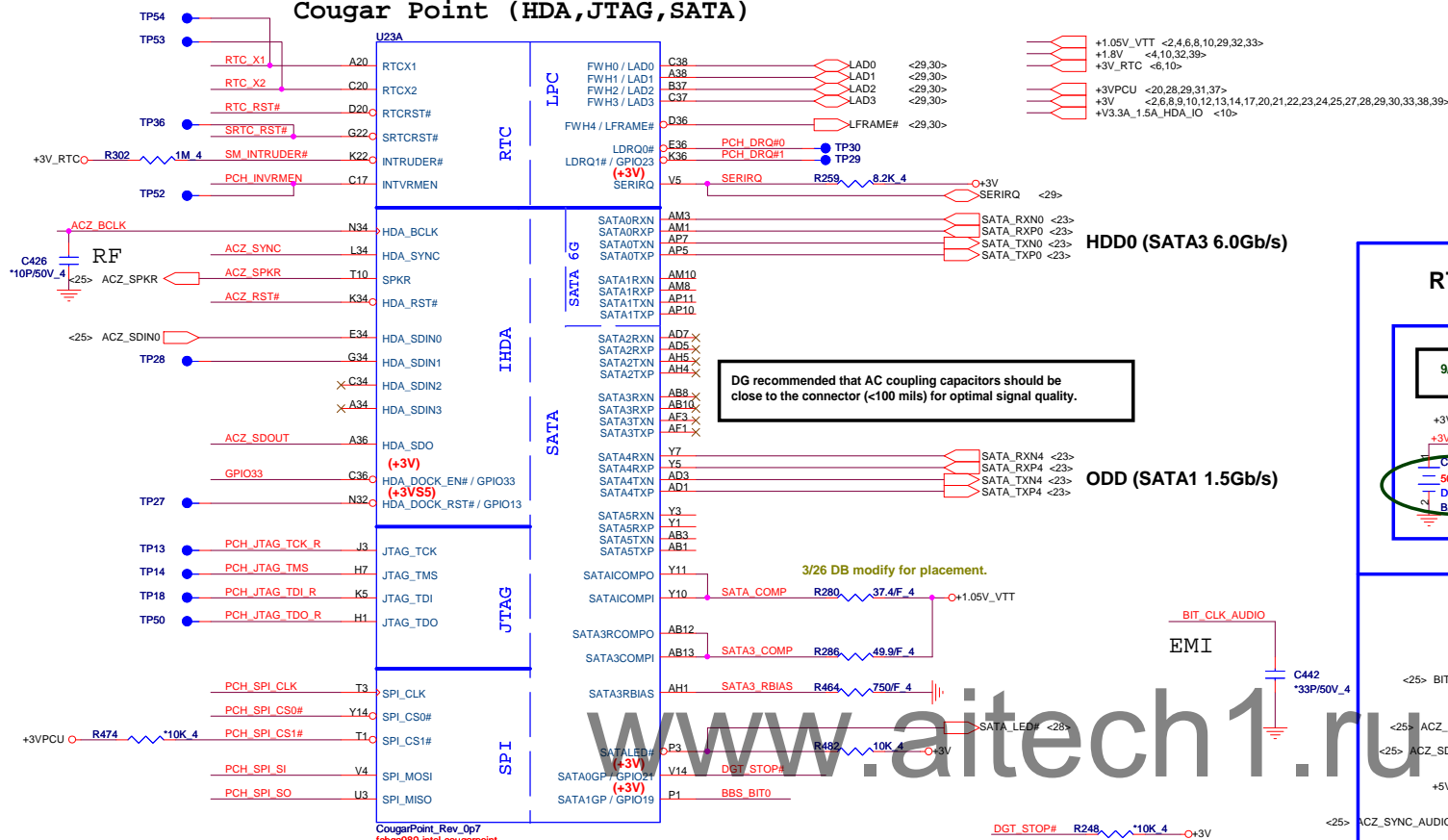


```
CFG[6:5] (PCIe Port Bifurcation Straps)
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```





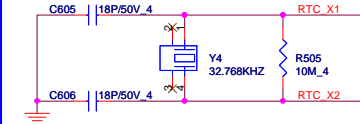
Cougar Point (HDA,JTAG,SATA)



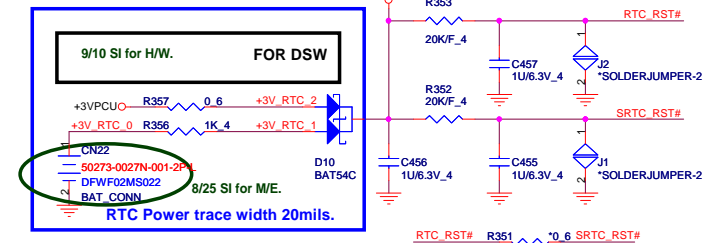
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R222 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R526 *1K 4 R525 10K 4 +3V PCI_GNT3# <8>
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R504 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R512 1K 4 GPIO33_E <29>
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R456 *1K 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R524 *1K 4 BBS_BIT1 <8>
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R476 *1K 4 NV_ALE <8>
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R477 2.2K 4 R478 4.7K 4 NV_CLE <8> N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R339 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDO R319 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R496 *1K 4 ICC_EN# <9>
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R219 *1K 4 PLL_ODVR_EN <9>
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R555 1K 4 +3V

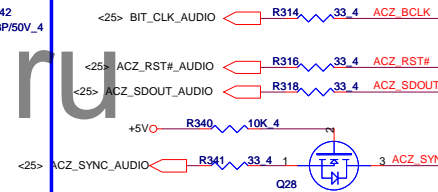
RTC Clock 32.768KHz



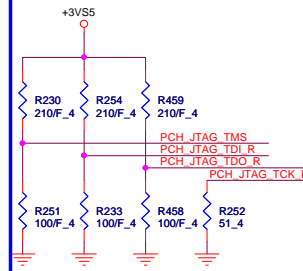
RTC Circuitry(RTC)



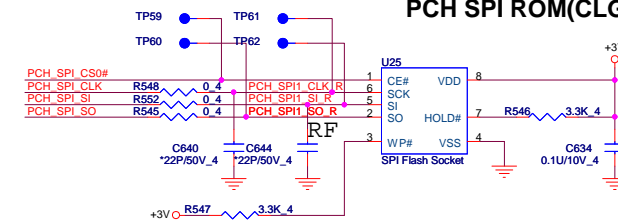
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

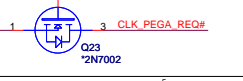
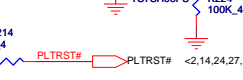
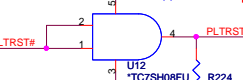
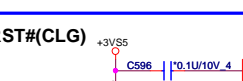
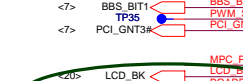
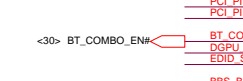
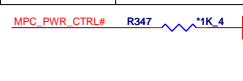
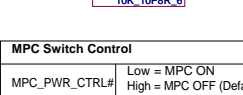
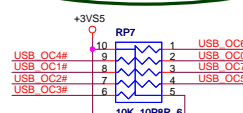
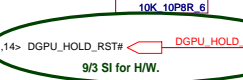
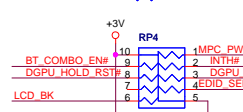
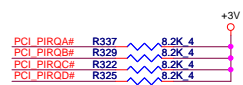


Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

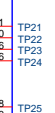
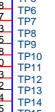
PROJECT : R13
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	3A
Date: Sunday, September 19, 2010	Sheet 7	of 39

PCI/USB0C# Pull-up(CLG)



U23E



U23B



U23A



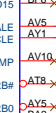
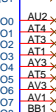
U23C



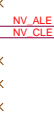
U23D



U23F



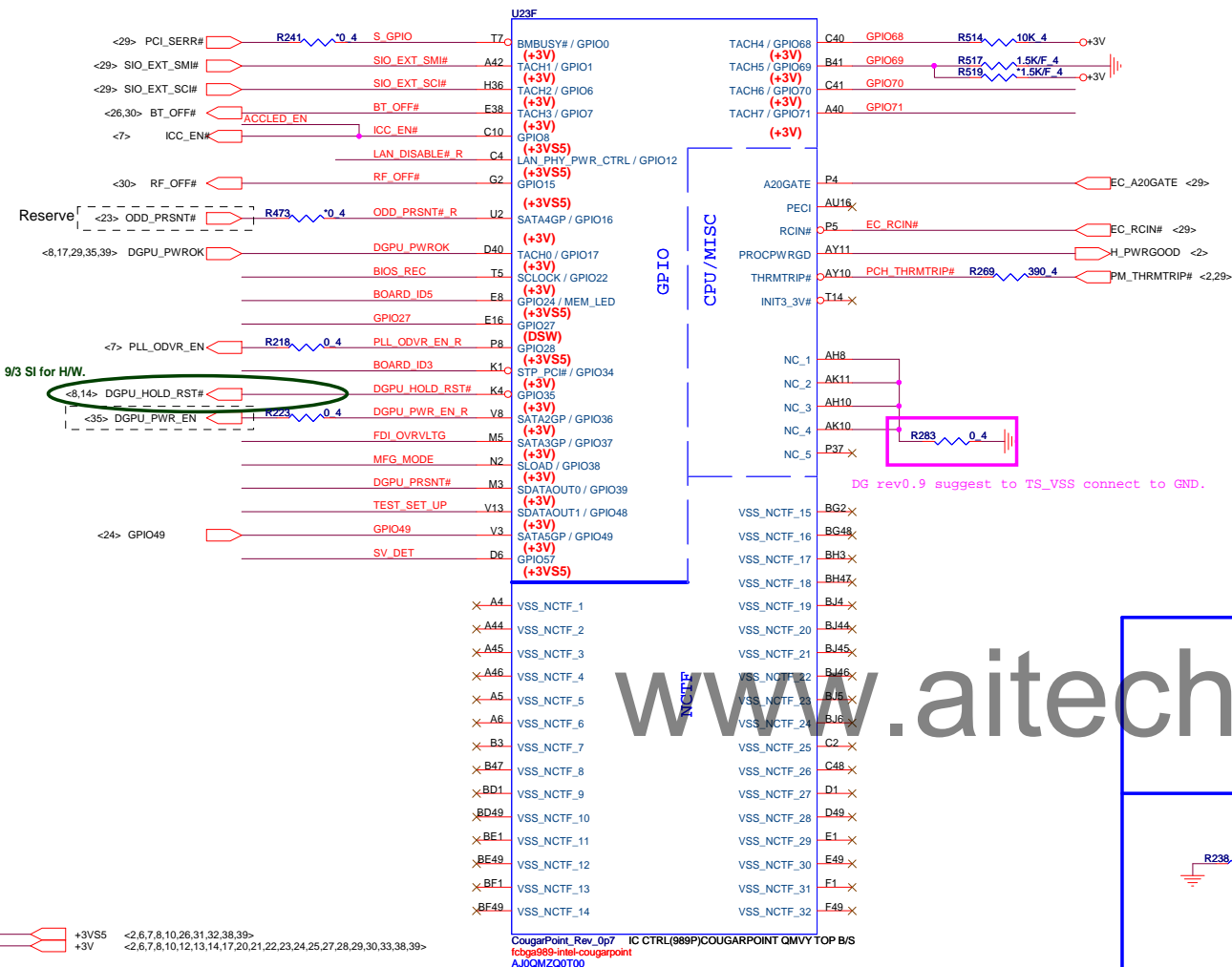
U23G



U23H

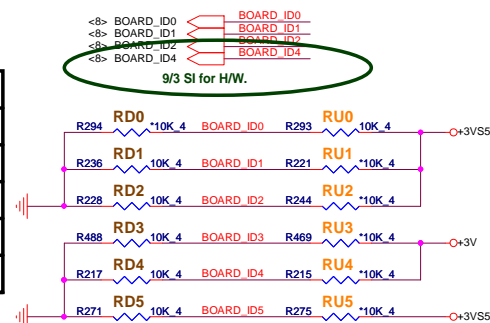


Cougar Point (GPIO,VSS_NCTF,RSVD)

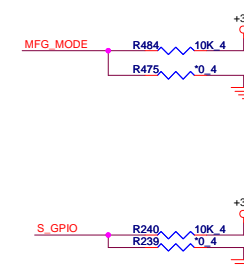


BOARD ID SETTING

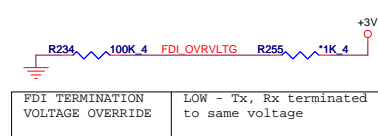
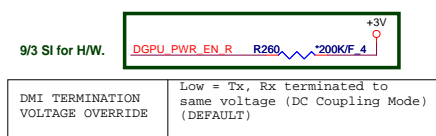
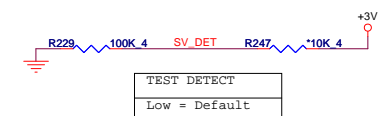
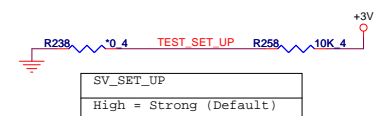
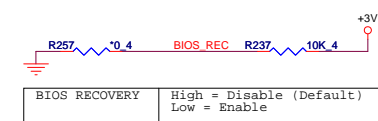
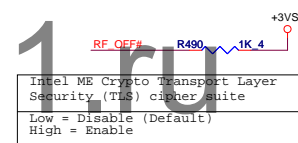
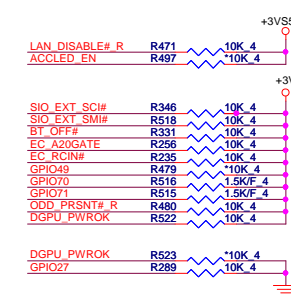
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R11 UMA	0	0	0	0	0	0
R11 DIS	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



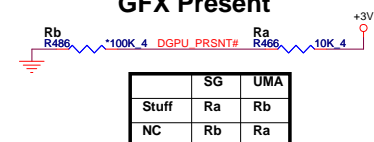
MFG-TEST



GPIO Pull-up/Pull-down(CLG)



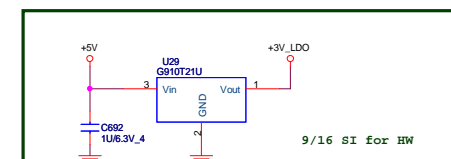
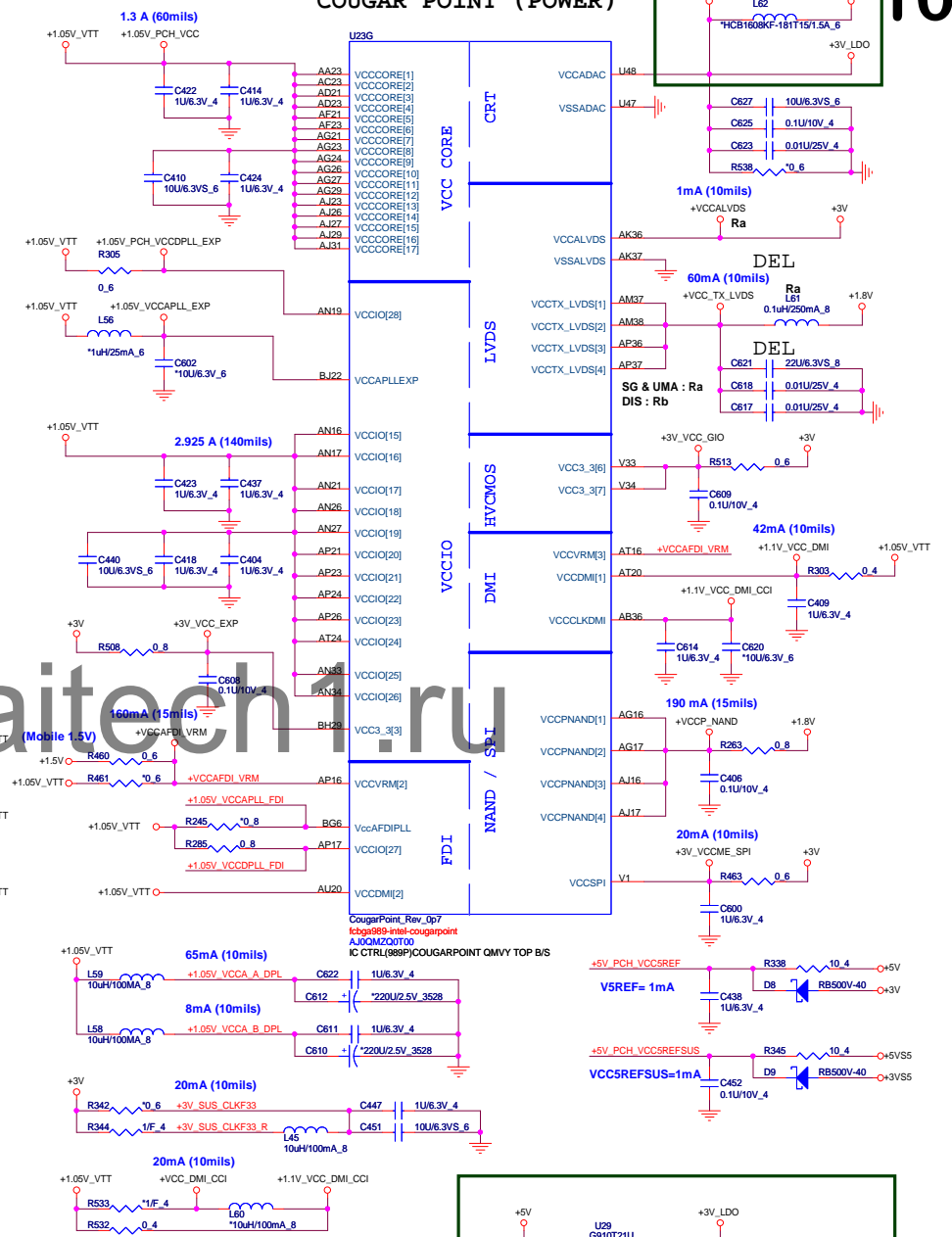
GFX Present



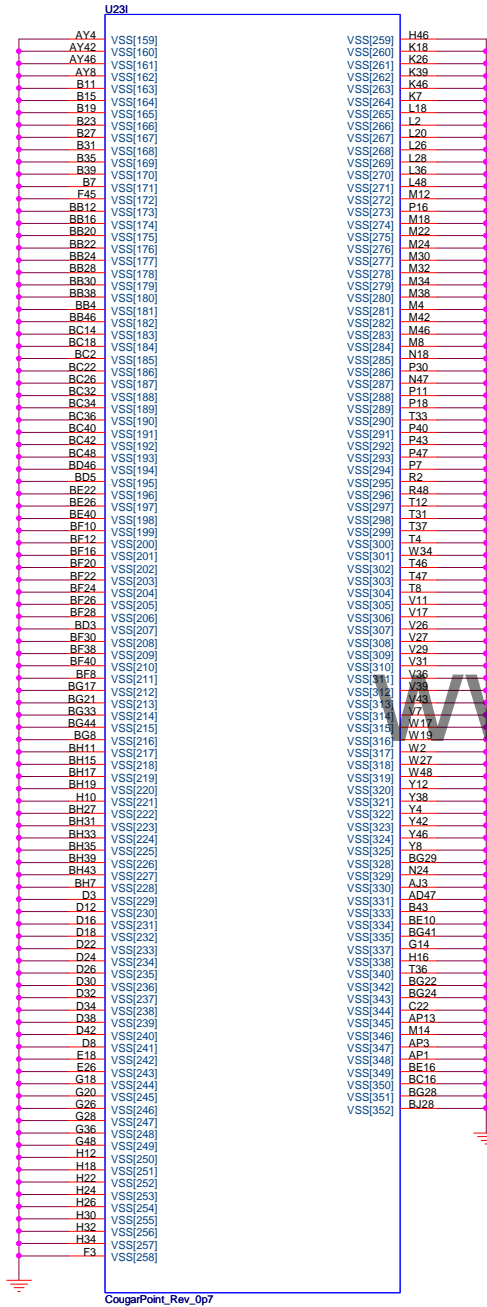
PROJECT : R13
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 3A
Date: Thursday, September 16, 2010 Sheet 9 of 39		

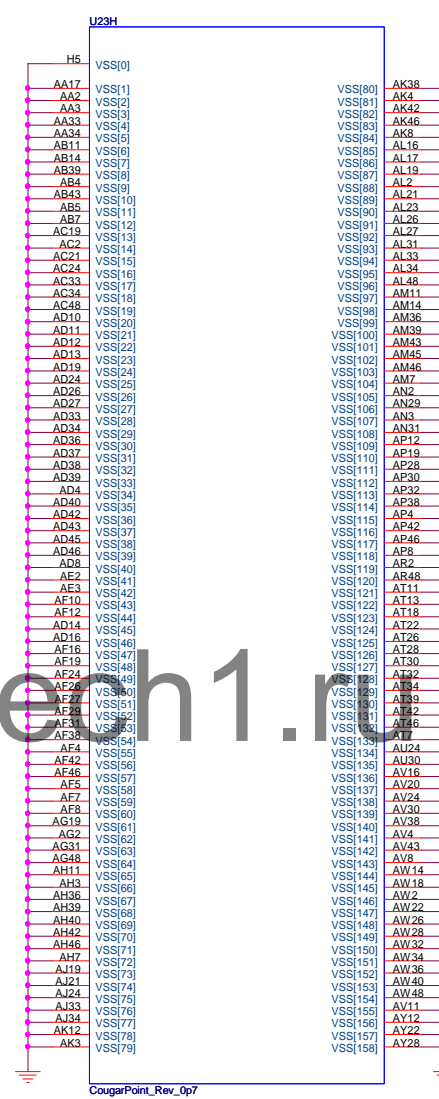
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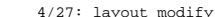
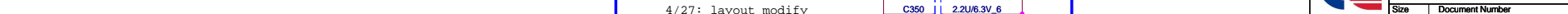


IBEX PEAK-M (GND)



IBEX PEAK-M (GND)





layout modify	C350	2.2U
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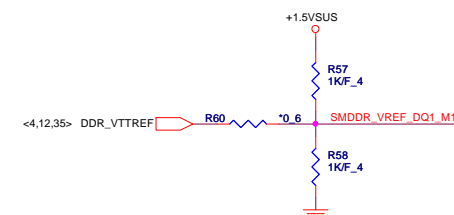


	Size	Document Num
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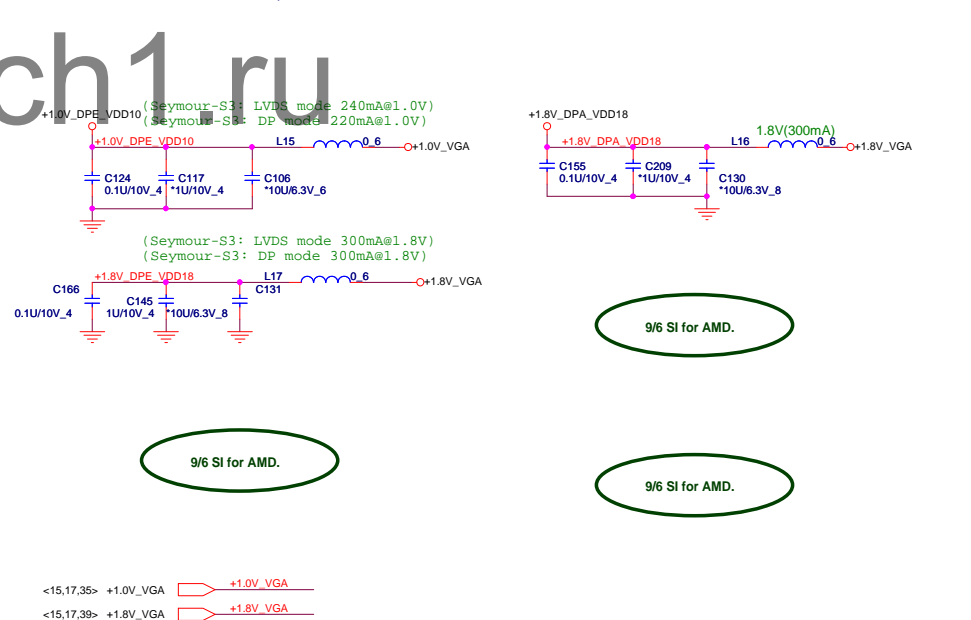
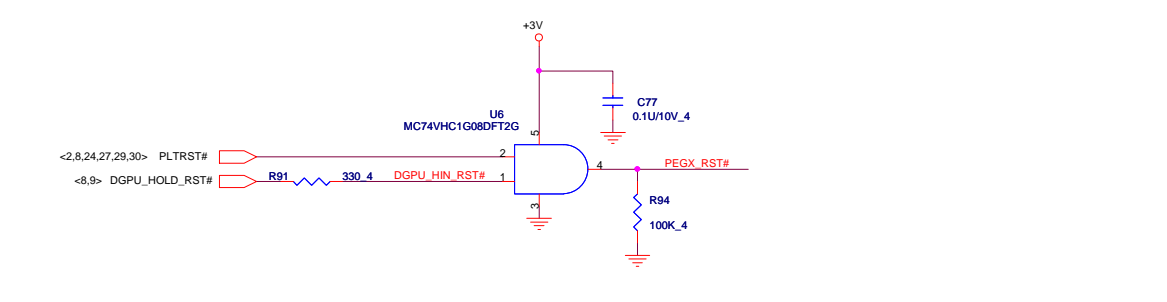


VREF DQ1 M1 Solution



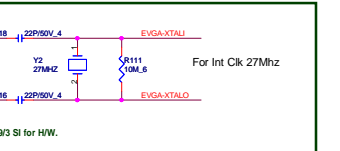
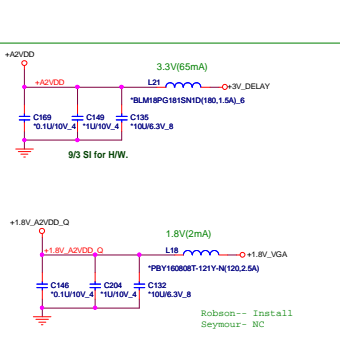
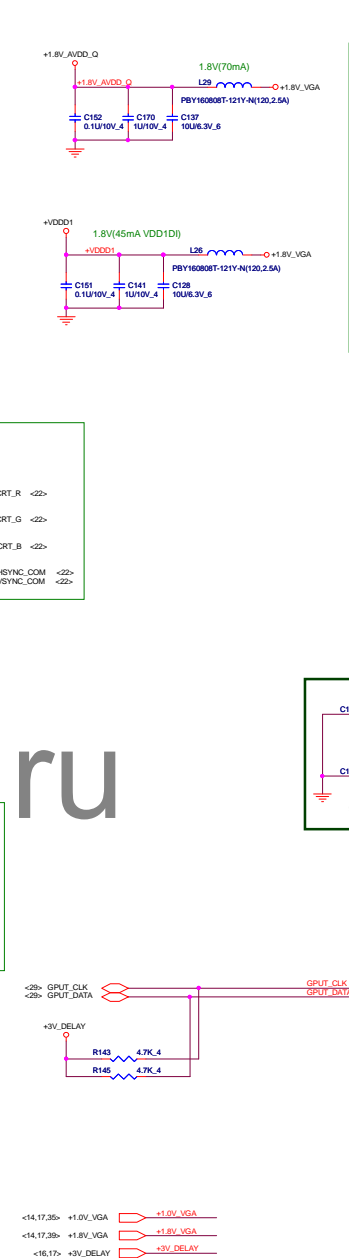
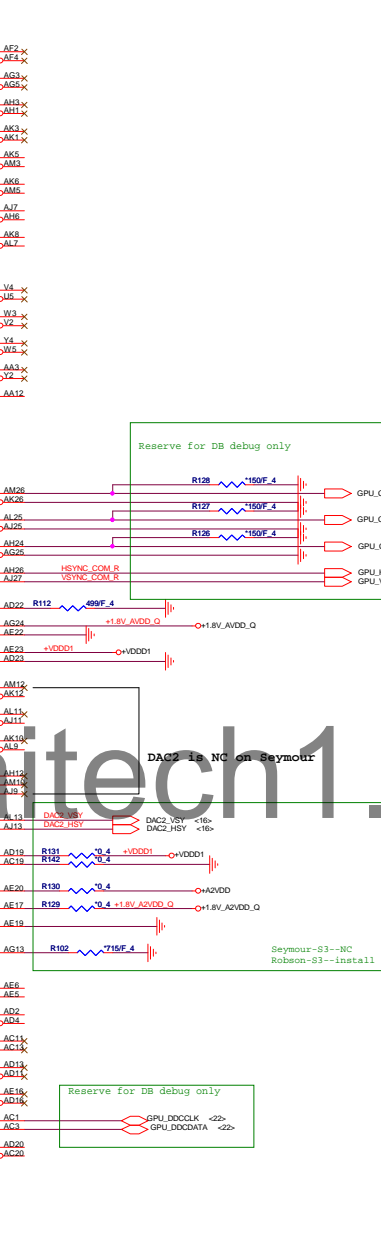
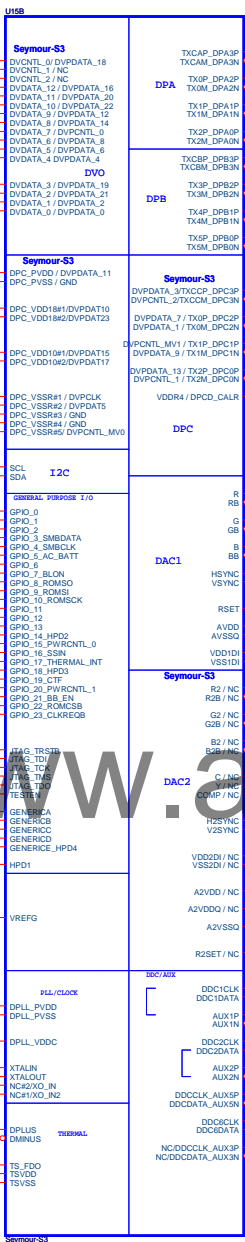
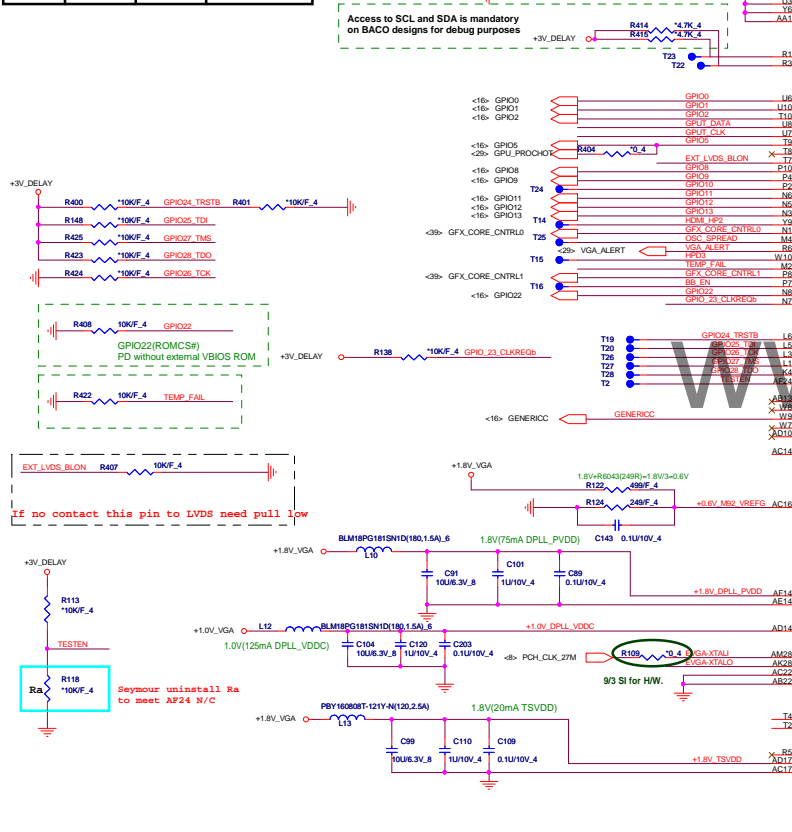
PROJECT :R11
Quanta Computer Inc.

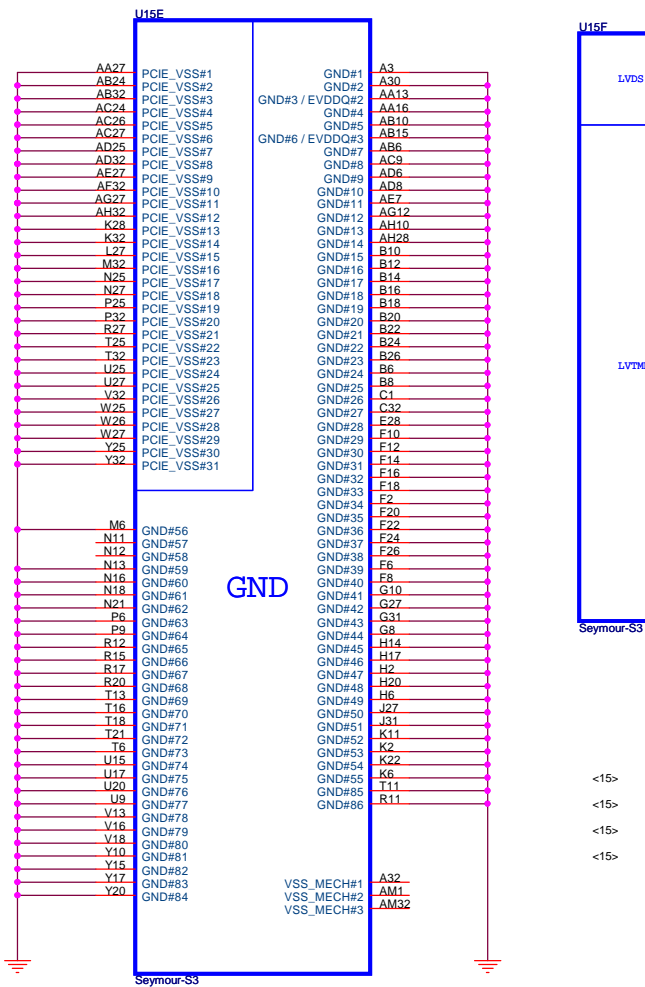
Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 1A
Date: Thursday, September 16, 2010 Sheet 13 of 39		



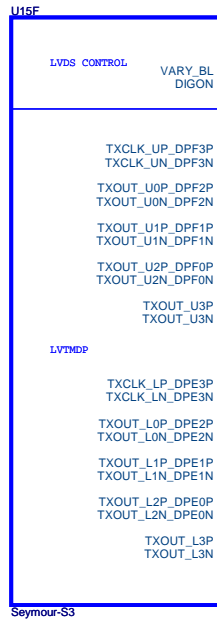
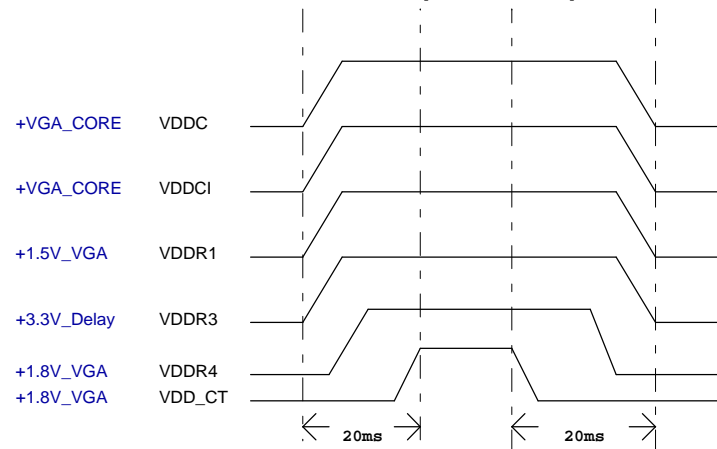
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung - E die	6416-8-900MHZ	K4W1G1646E-HC12
0001	Hynix - Vega die	12816-8-900MHZ	H5G42G1646C-12C
0010	Hynix - Vega die	12816-8-900MHZ	H5G42G1646C-12C
0011	Hynix - Vega die	12816-8-900MHZ	H5G42G1646C-12C
0100	Microton	12816-8-900MHZ	K4W1G1646E16A-125D
0101	Microton	12816-8-900MHZ	K4W1G1646E16A-125D
0110	Hynix - Vega die	12816-8-900MHZ	K4W1G1646E-HC12
0111	Hynix - Vega die	12816-8-900MHZ	K4W1G1646E-HC12
1000	Samsung - G die	12816-8-900MHZ	Reserved
1001	Samsung - G die	12816-8-900MHZ	Reserved
1010	Hynix - Vega die	12816-8-900MHZ	Reserved
1011	Hynix - Vega die	12816-8-900MHZ	Reserved
1100	Samsung - G die	12816-8-900MHZ	Reserved
1101	Samsung - G die	12816-8-900MHZ	Reserved
1110	Samsung - G die	12816-8-900MHZ	Reserved
1111	Samsung - G die	12816-8-900MHZ	Reserved

GPIO15 GPIO20			
Seymour	PWRCTRL0	PWRCTRL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (default)
TBD	1	1	NA

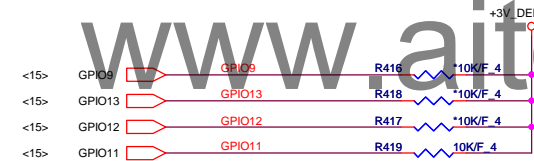




Power Up/Down Sequence



Seymour-S3



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

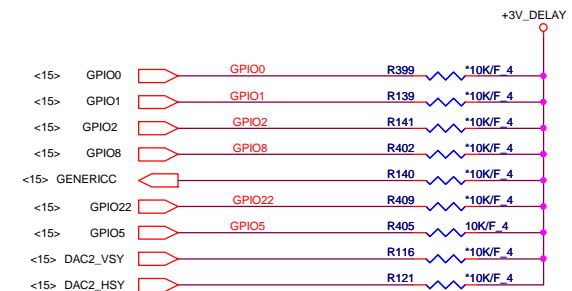
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	



PROJECT :R11
Quanta Computer Inc.



U_PWROK

Q19 2N7002

Q8 2N7002

Q7 2N7002

U3 TC7SH08FU

C53 0.1uF/10V_4

R44 1K_4

R68 1K_4

BACO_EN

PX_EN#

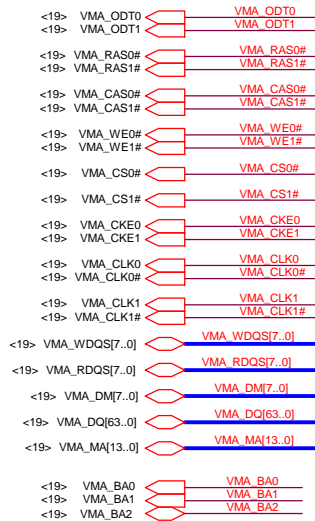
PX_EN#

Netel.

1. No BACO Support :BIF_VDDC s
2. BACO Support: Refer to the schematics/Application note for if BACO is Supported (Uninstall

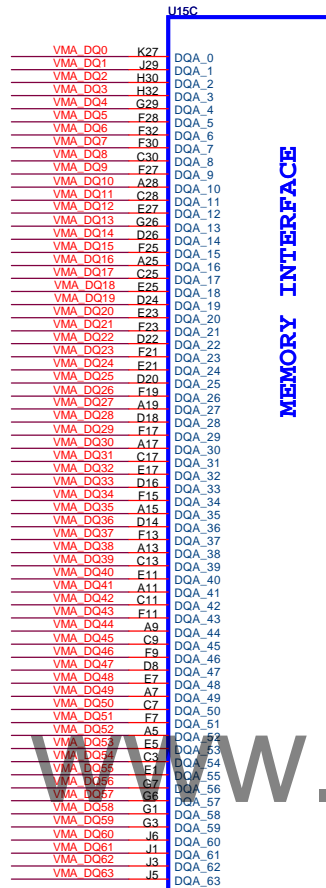
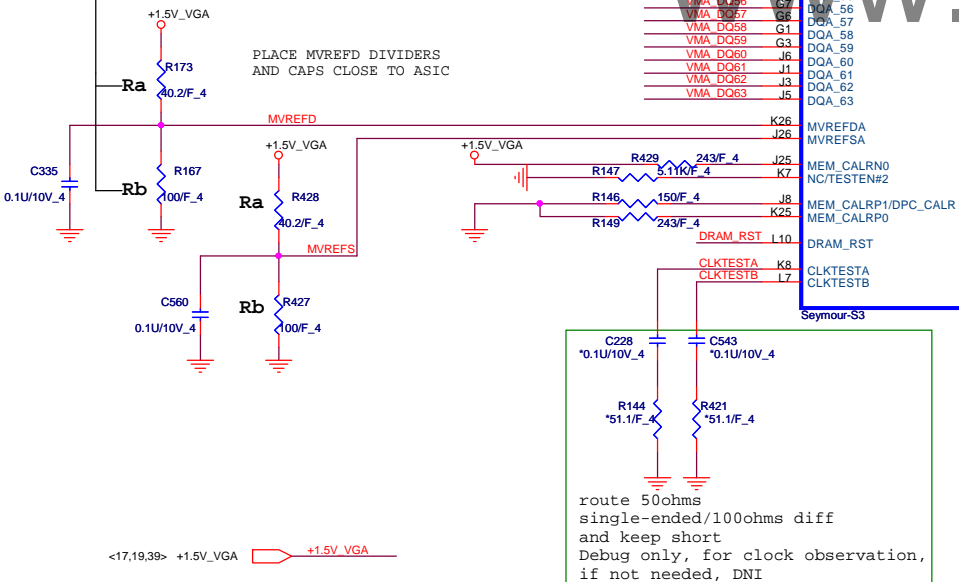


Size Custom	Document Number Seymour_Power_and_NC	Rev 1A
Date: Thursday, September 16, 2010		Sheet 17 of 39

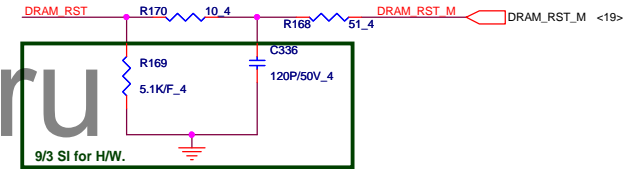
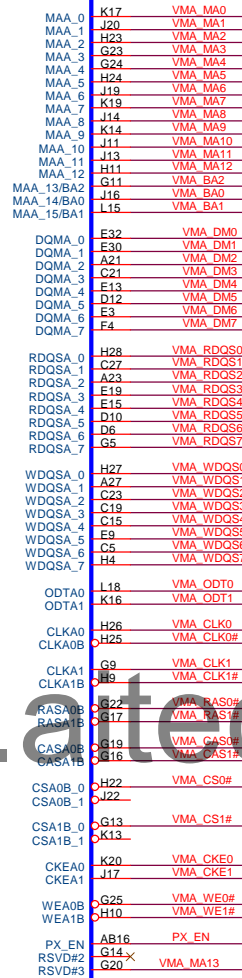


support 1Gbit
VRAM (64K X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

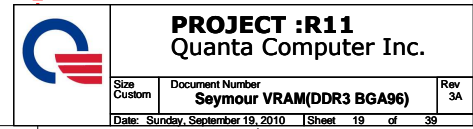


MEMORY INTERFACE



PROJECT :R11
Quanta Computer Inc.

Size Custom	Document Number Seymour/MEM_Interface	Rev 1A
Date: Thursday, September 16, 2010	Sheet 18	of 39



20



<2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,33,38,39> +3V
 <7,28,29,31,37> +3VPCU
 <6,7,10,17,21,22,23,25,28,30,38> +5V
 <23,37,38,39> +12VALW
 <31,32,34,35,36,37,38,39> +VIN

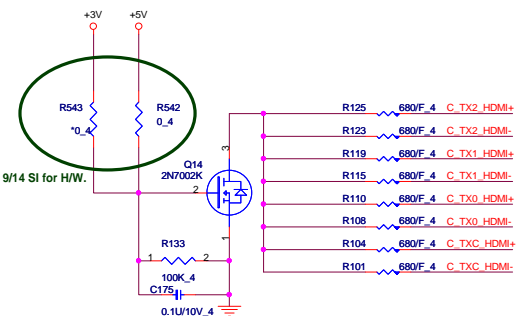


Size Custom	Document Number LCD CONN/LID/CAM	Rev 1A
Date: Sunday, September 19, 2010		Sheet 20 of 39

close to HDMI conn

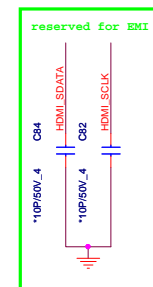
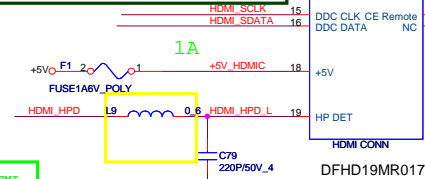
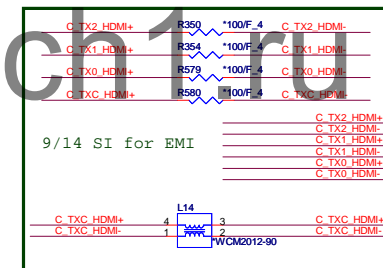
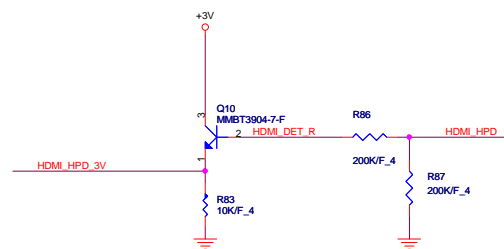
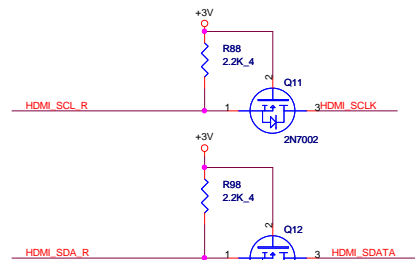
	IN_CLK#	IN_CLK#	C98	0.1U/10V_4	C.TXC.HDMI-
	IN_CLK	IN_CLK	C105	0.1U/10V_4	C.TXC.HDMI+
	IN_D0#	IN_D0#	C115	0.1U/10V_4	C.TX0.HDMI-
	IN_D0	IN_D0	C121	0.1U/10V_4	C.TX0.HDMI+
	IN_D1#	IN_D1#	C125	0.1U/10V_4	C.TX1.HDMI-
	IN_D1	IN_D1	C129	0.1U/10V_4	C.TX1.HDMI+
	IN_D2#	IN_D2#	C142	0.1U/10V_4	C.TX2.HDMI-
	IN_D2	IN_D2	C153	0.1U/10V_4	C.TX2.HDMI+

<6> SDVO_CLK SDVO_CLK HDMI_SCL_R
 <6> SDVO_DATA SDVO_DATA HDMI_SDA_R
 <6> HDMI_HPD_CON HDMI_HPD_CON HDMI_HPD_3V

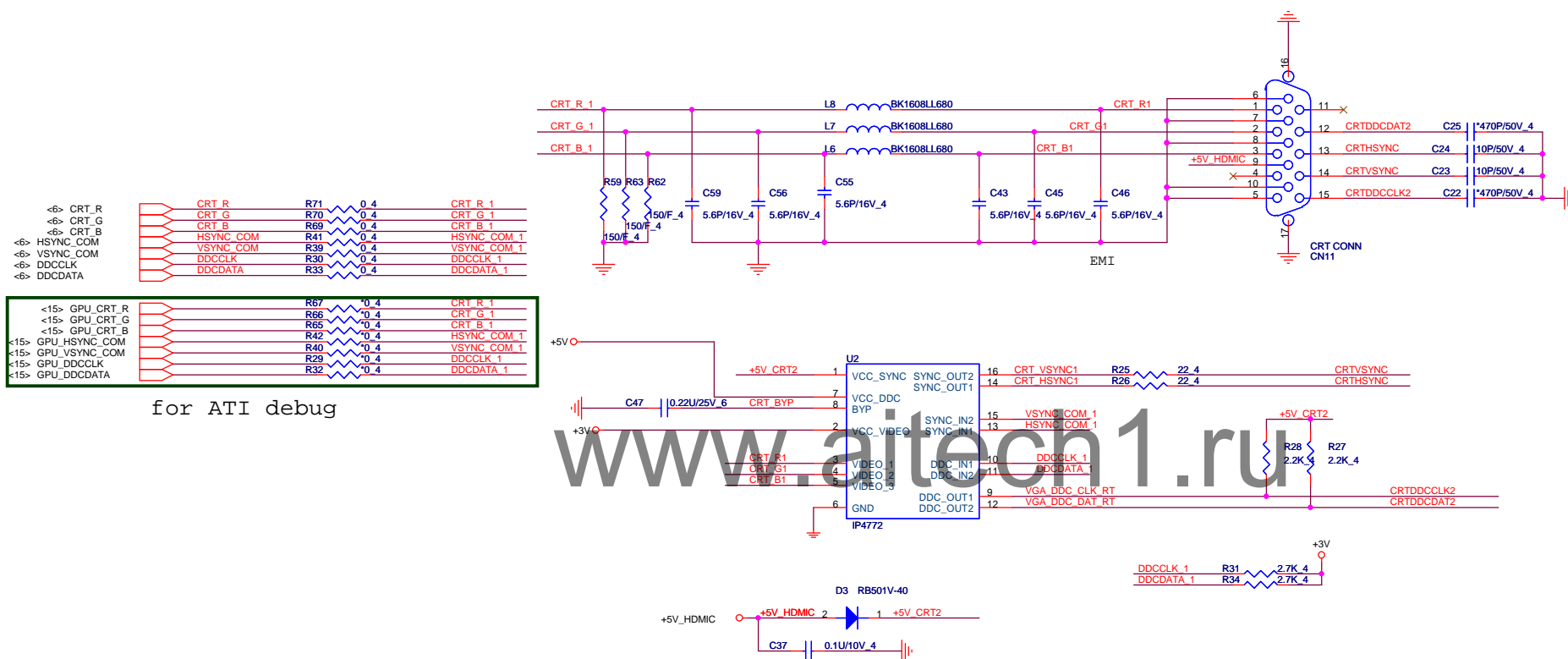


DISCRETE HDMI I2C SELECT

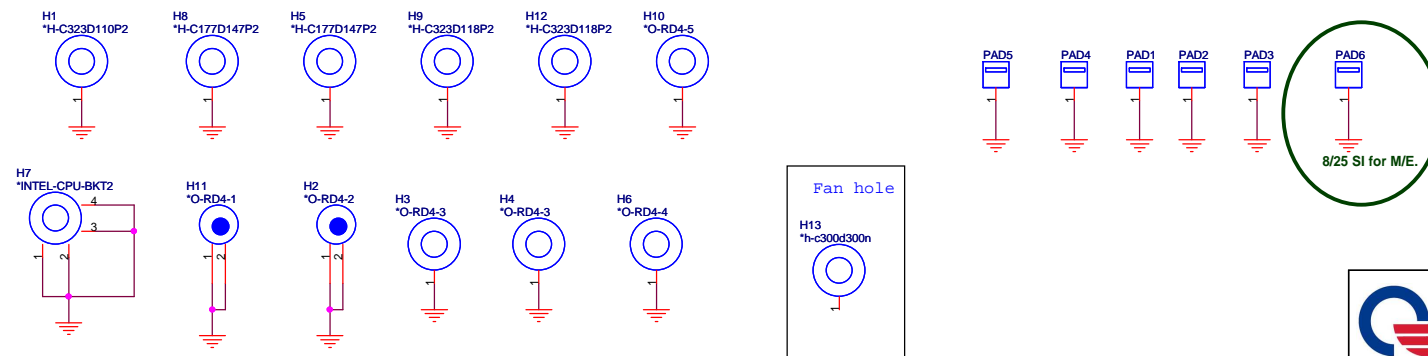
Close to HDMI Connector



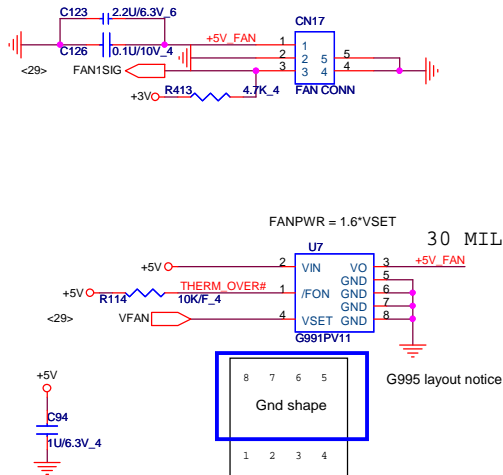
CRT PORT



Hole

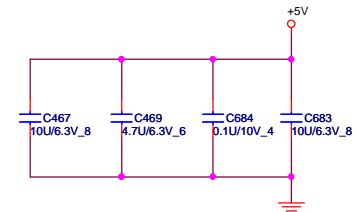
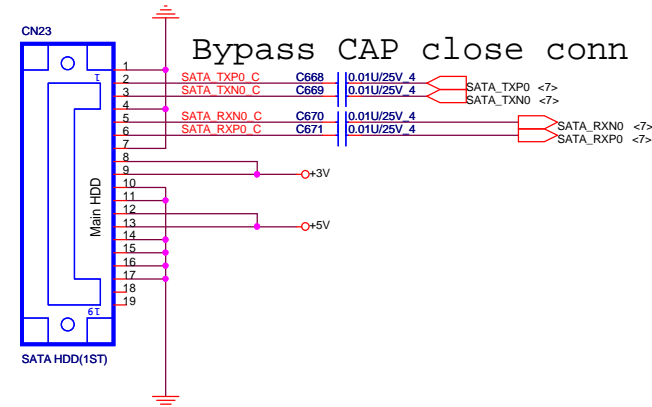


CPU FAN

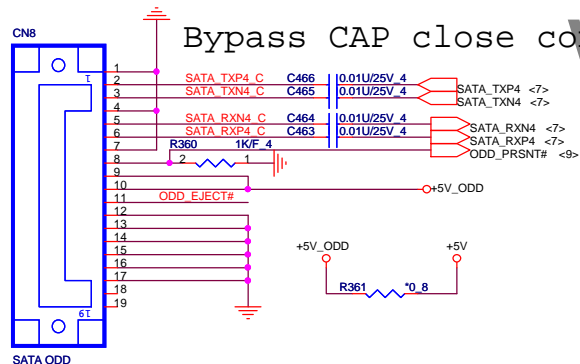


SATA HDD CONNECTOR

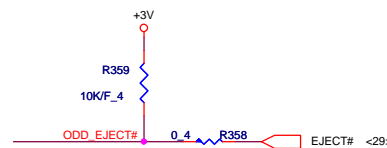
23



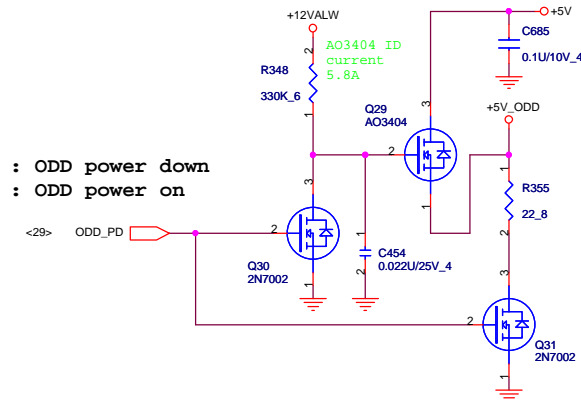
SATA ODD CONNECTOR



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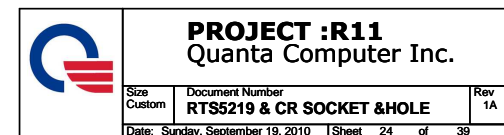


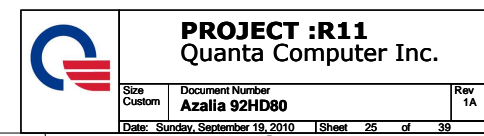
High : ODD power down
Low : ODD power on



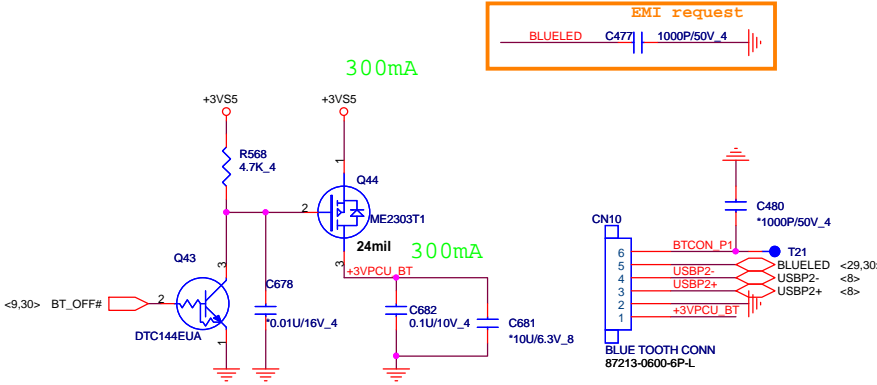
PROJECT :R11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A
Date:	Sunday, September 19, 2010	Sheet 23 of 39

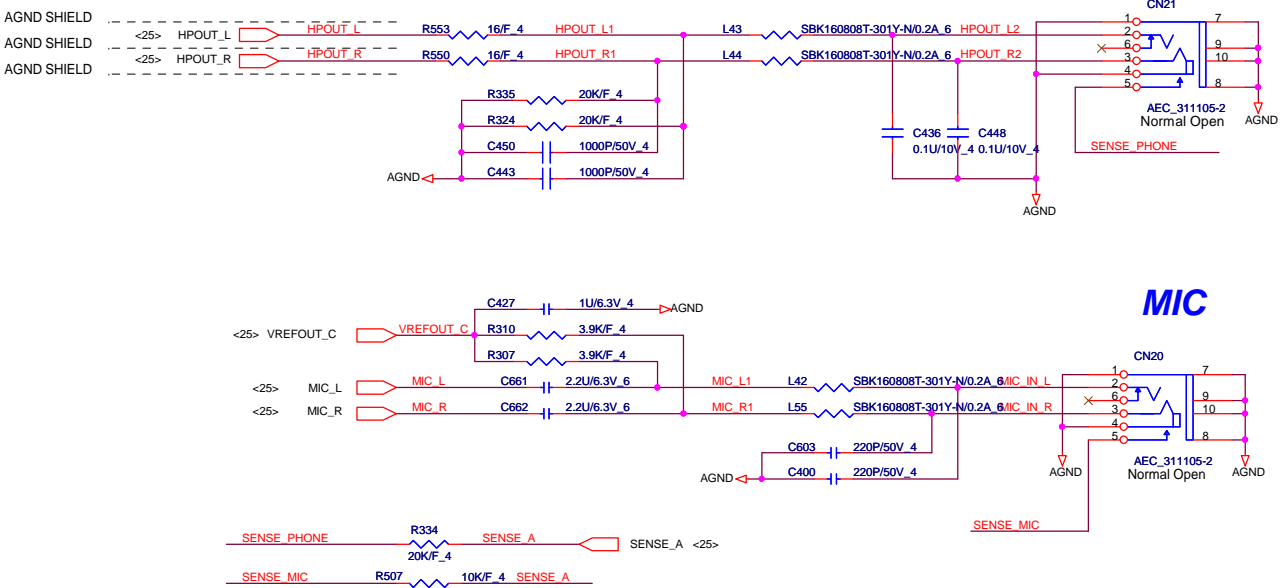
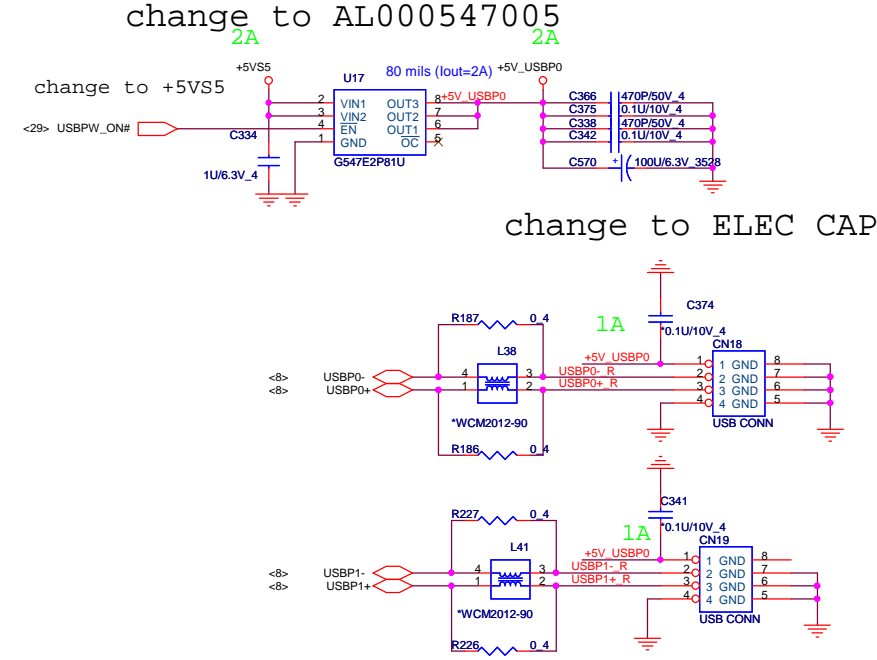




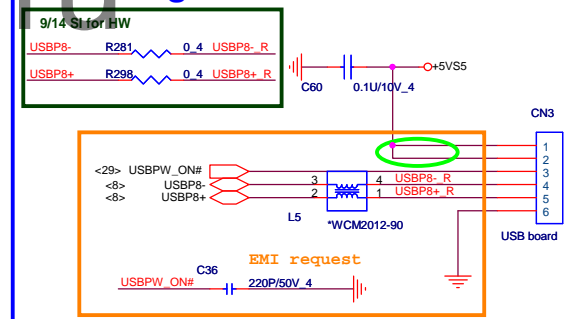
BLUETOOTH



LEFT SIDE USBX2

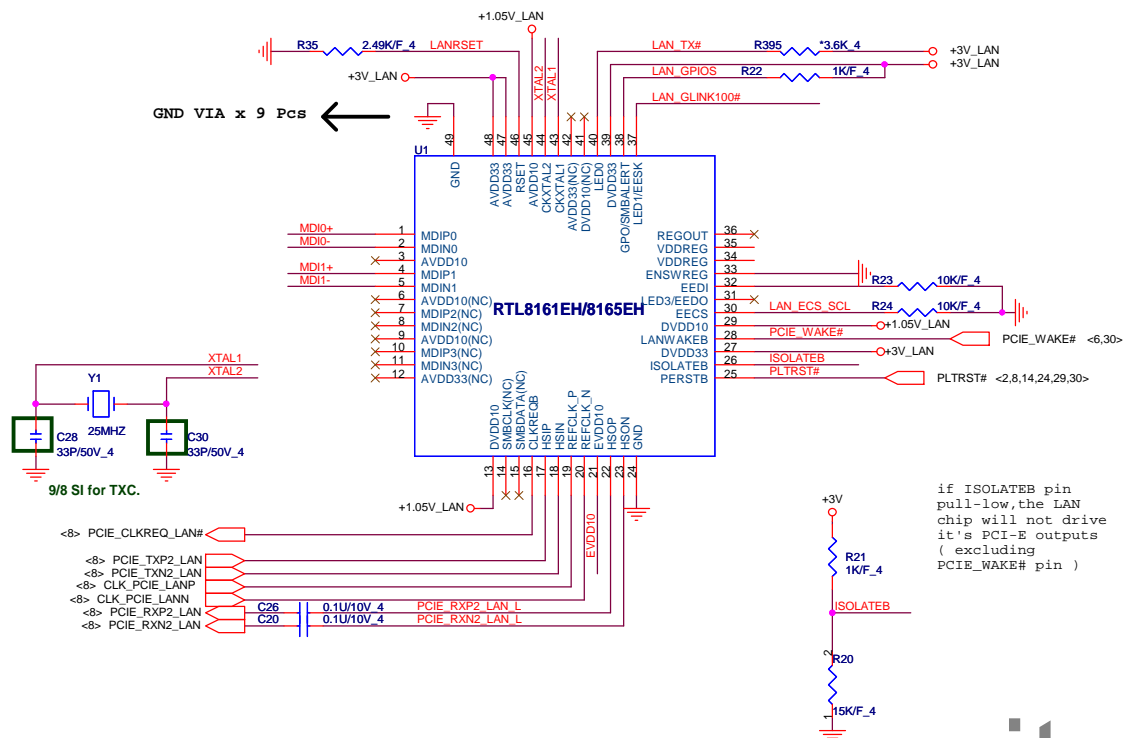


Right SIDE USBX1



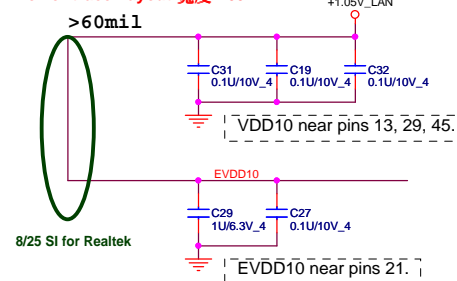
PROJECT :R11
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	USB/BT/Audio Jack	
Date: Monday, September 20, 2010	Sheet 26 of 39	

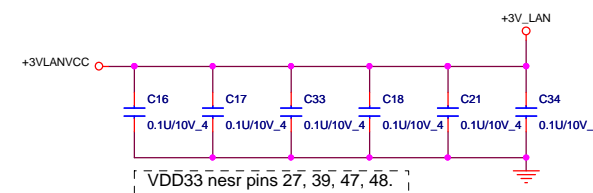
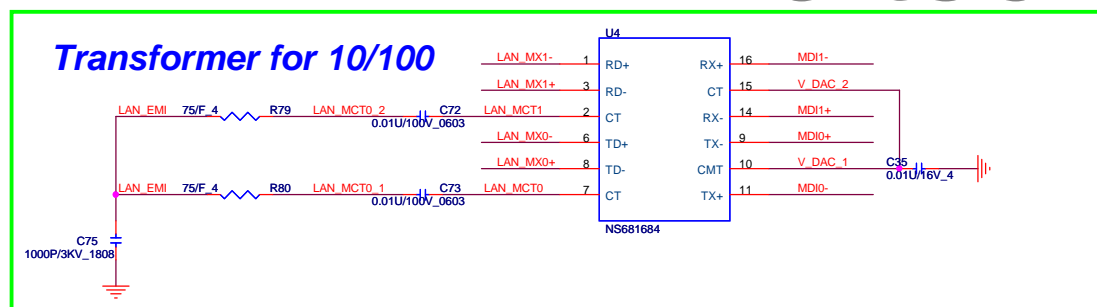


IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

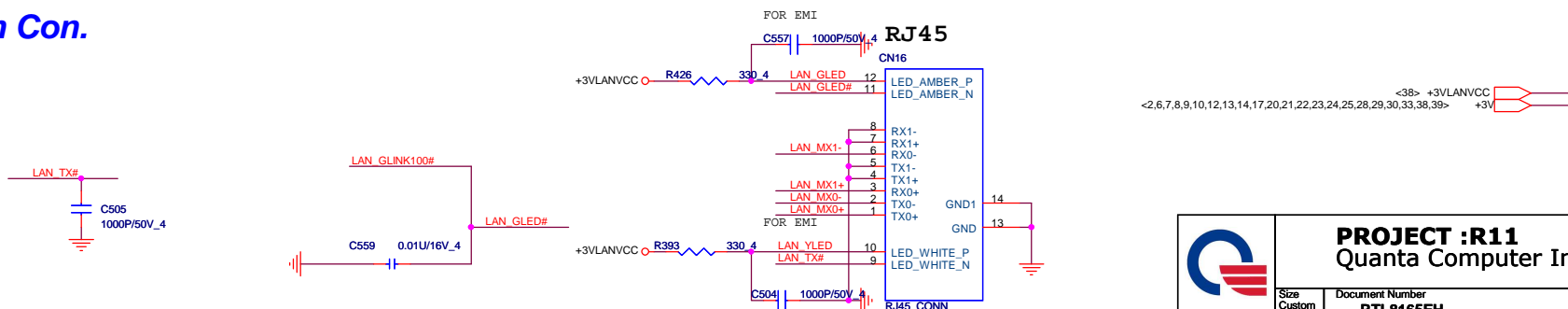
Power trace Layout 寬度> 60mil



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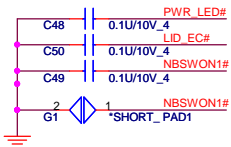
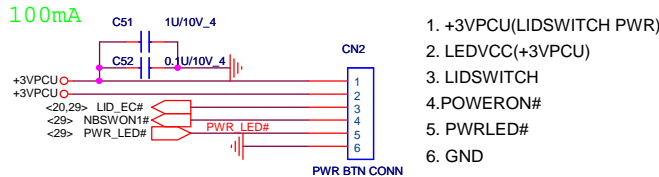
Lan Con.



PROJECT :R11
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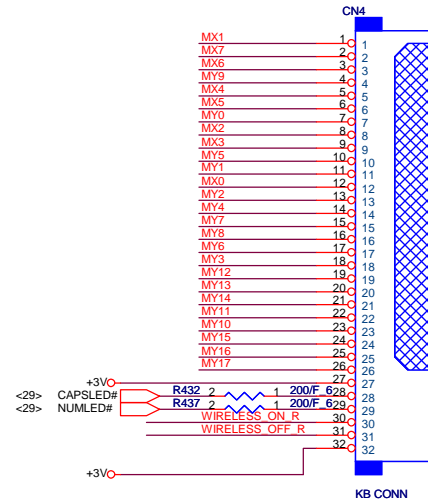
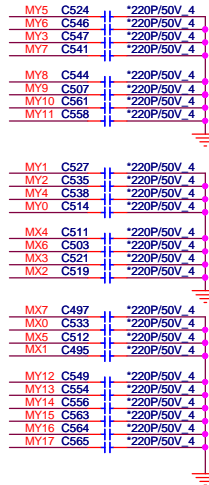
Size Custom	Document Number RTL8165EH
Date: Sunday, September 19, 2010	Sheet 27 of 39

POWER BOTTON CONNECT



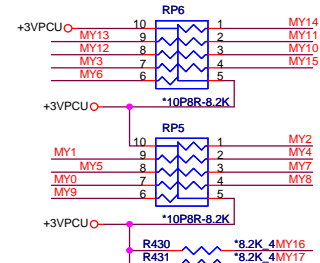
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.



EC KB3930 has included K/B pull-up resistor and function

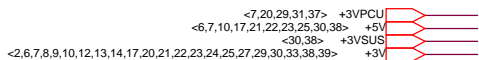
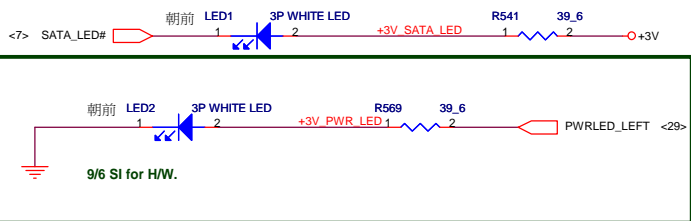
KEYBOARD PULL-UP



28

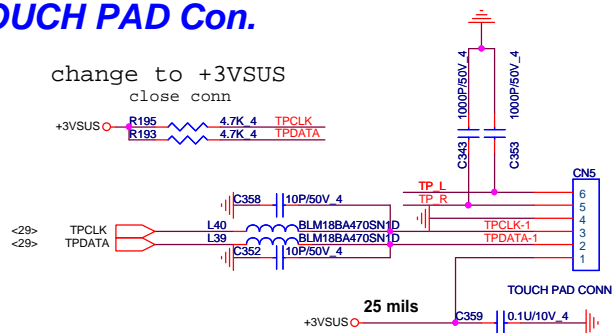


LED

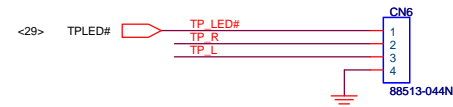


TOUCH PAD Con.

```
change to +3VSUS
      close conn
```

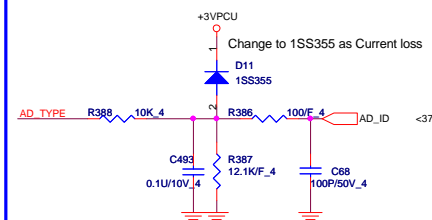


To TOUCH PAD SW board

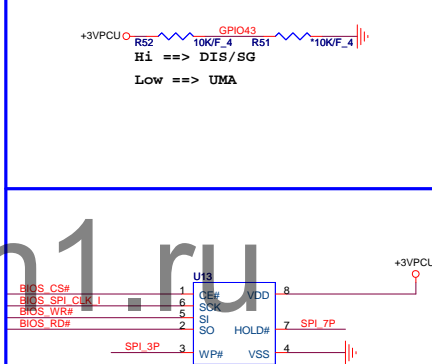


PROJECT :R11
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Size Custom	Document Number LED/KB/SW/TP	R
Date: Thursday, September 16, 2010		Sheet 28 of 39



512K byte SPI EC ROM

[illegible]

+3VPCU ○

Resistor	Value	Signal
R95	10K/F_4	NBSWON1#
R372	4.7K_4	MBCLK
R370	4.7K_4	MBDATA

Change to RB500 as Current loss

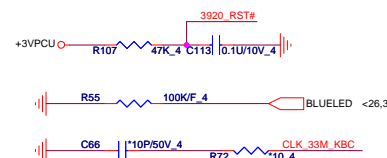
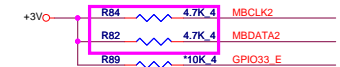
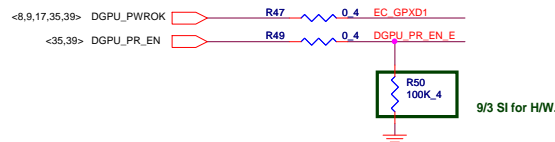
SCI1# D5 1 2 RB501V-40 SIO_EXT_SCI# <9

DNBSWON#1 D4 1 2 RB500V-40 DNBSWON# <6

KBSM1# D7 1 2 RB500V-40 SIO_EXT_SM# <9

Add Pin 117,103 for DSM,116 for Bluetooth

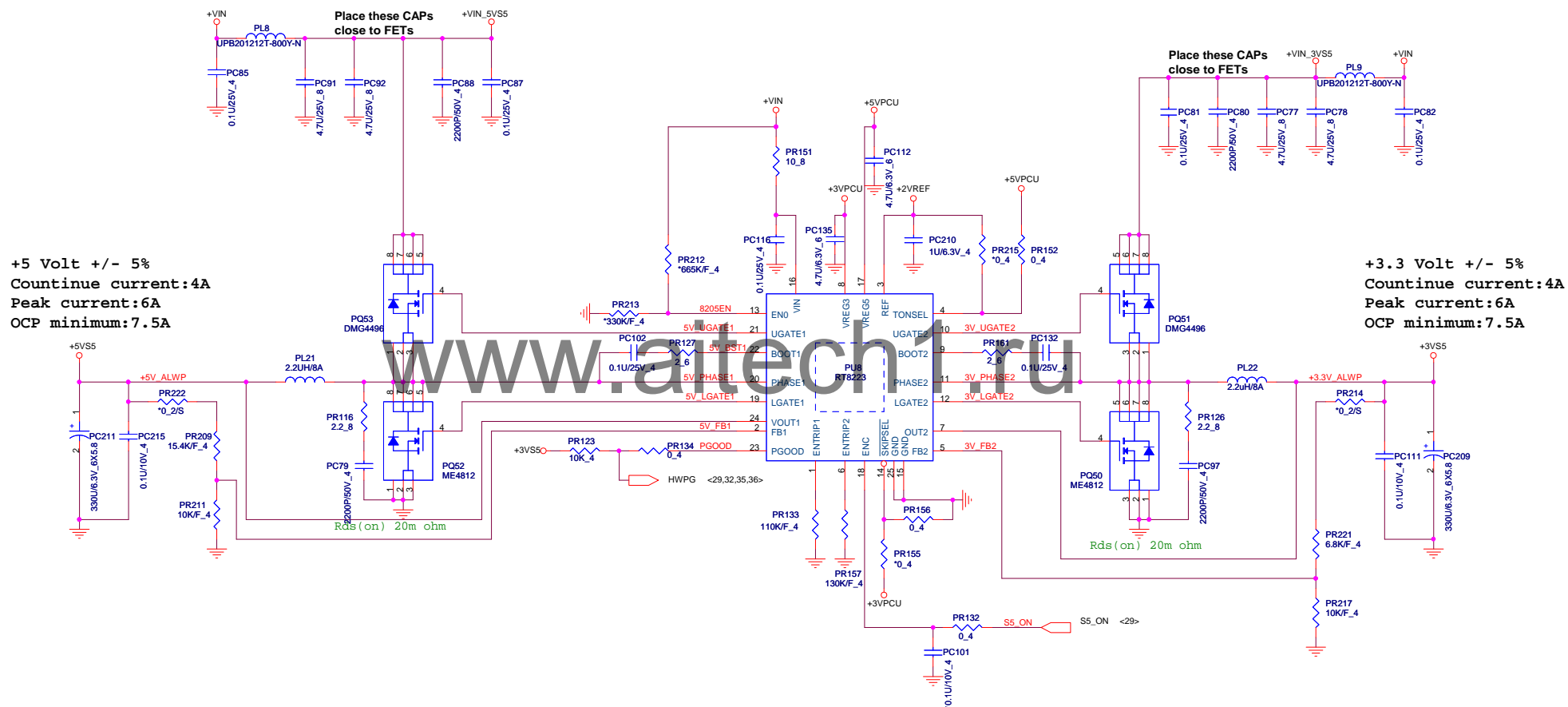
Delete T10 and tie pin 117 from Lan for DSM

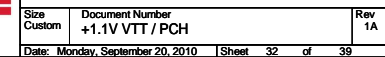
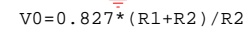


30

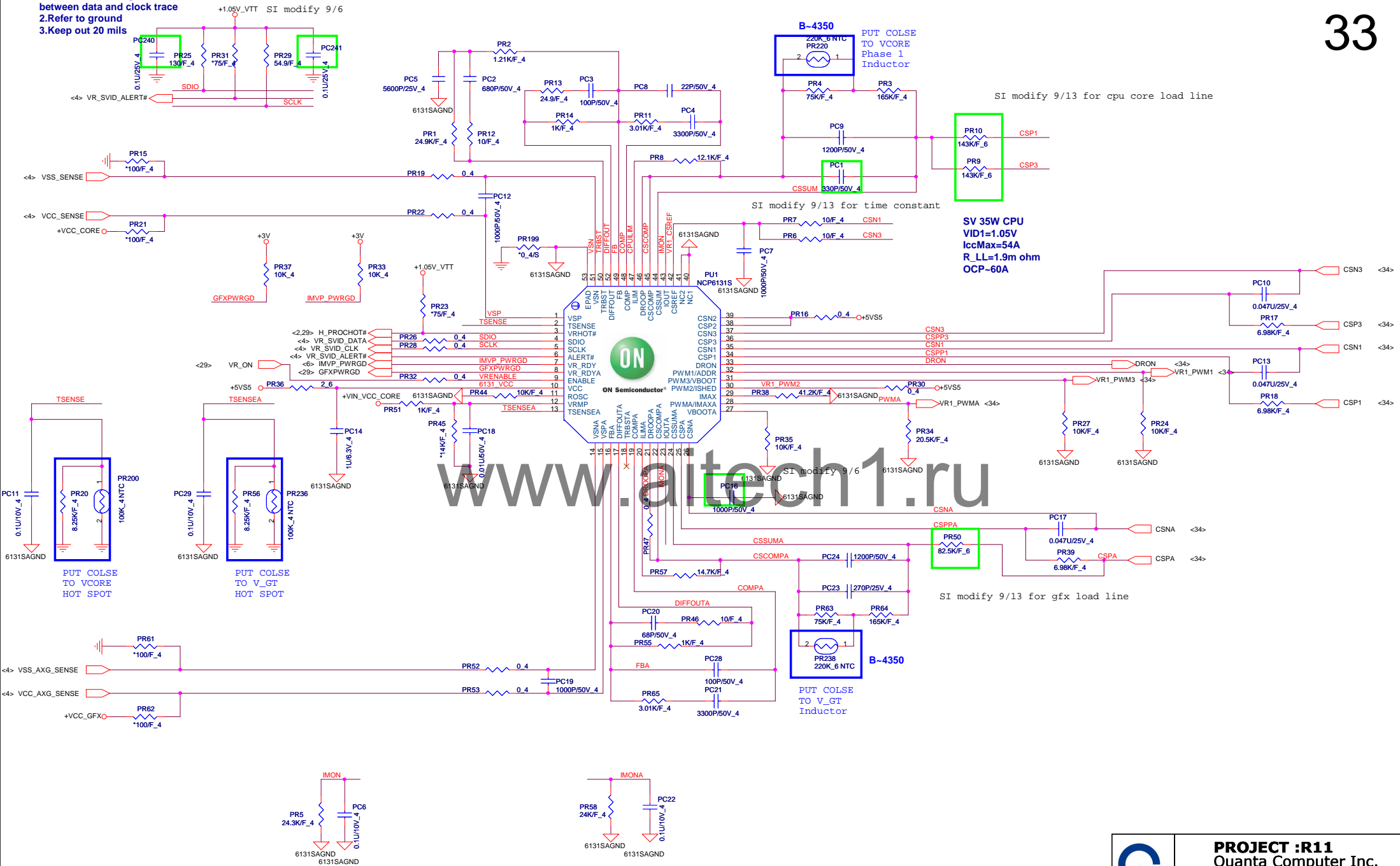


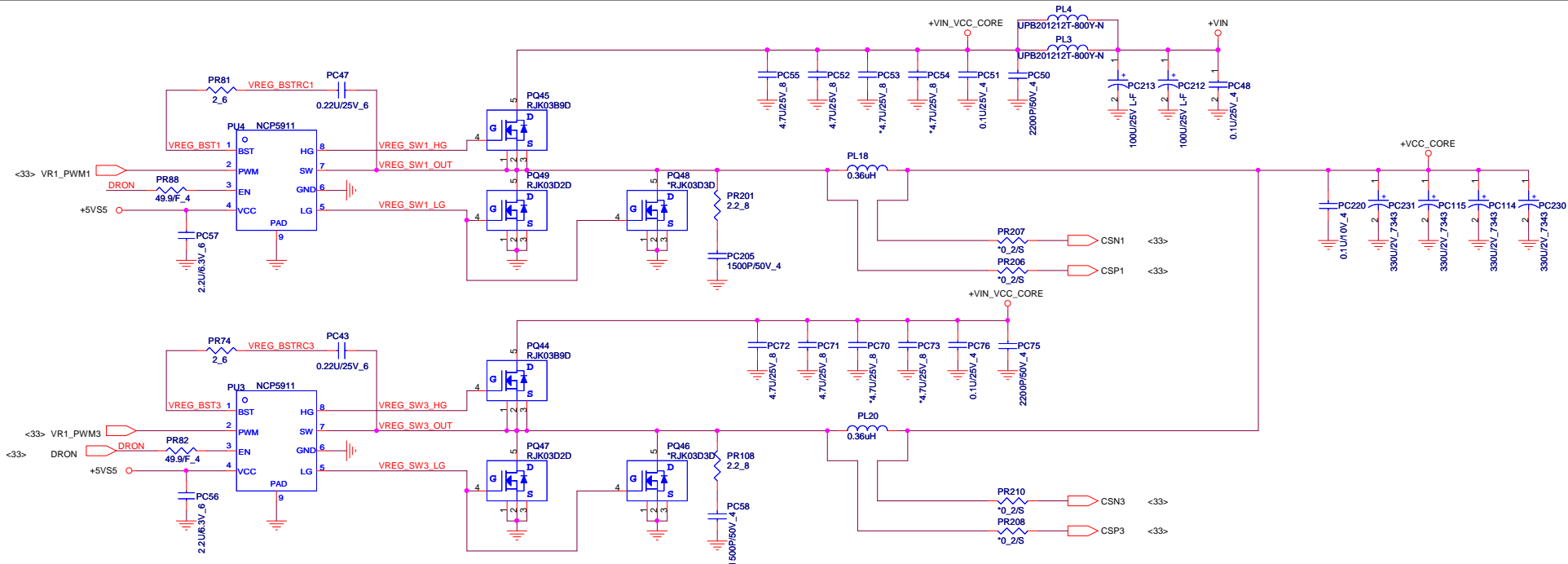
DC/DC +3VS5/+5VS5



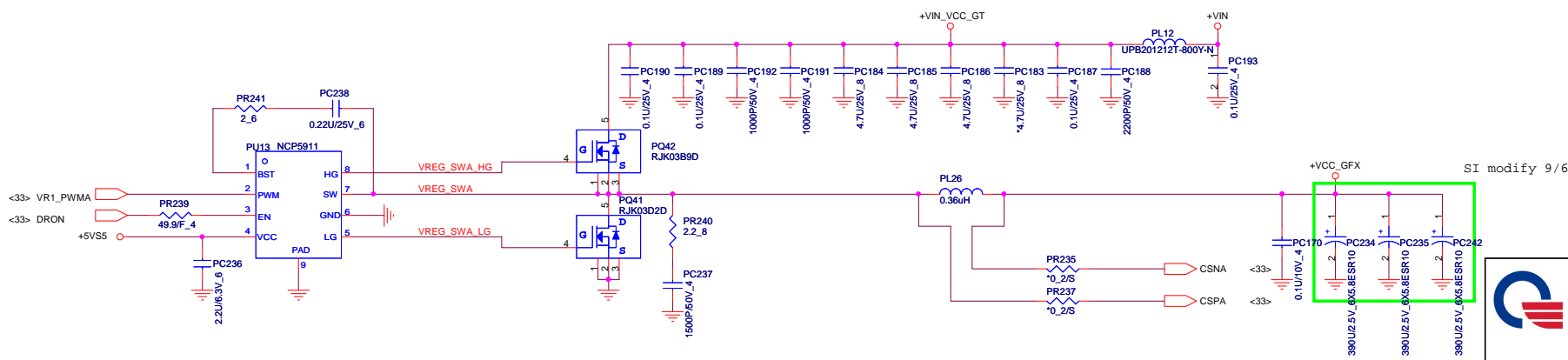


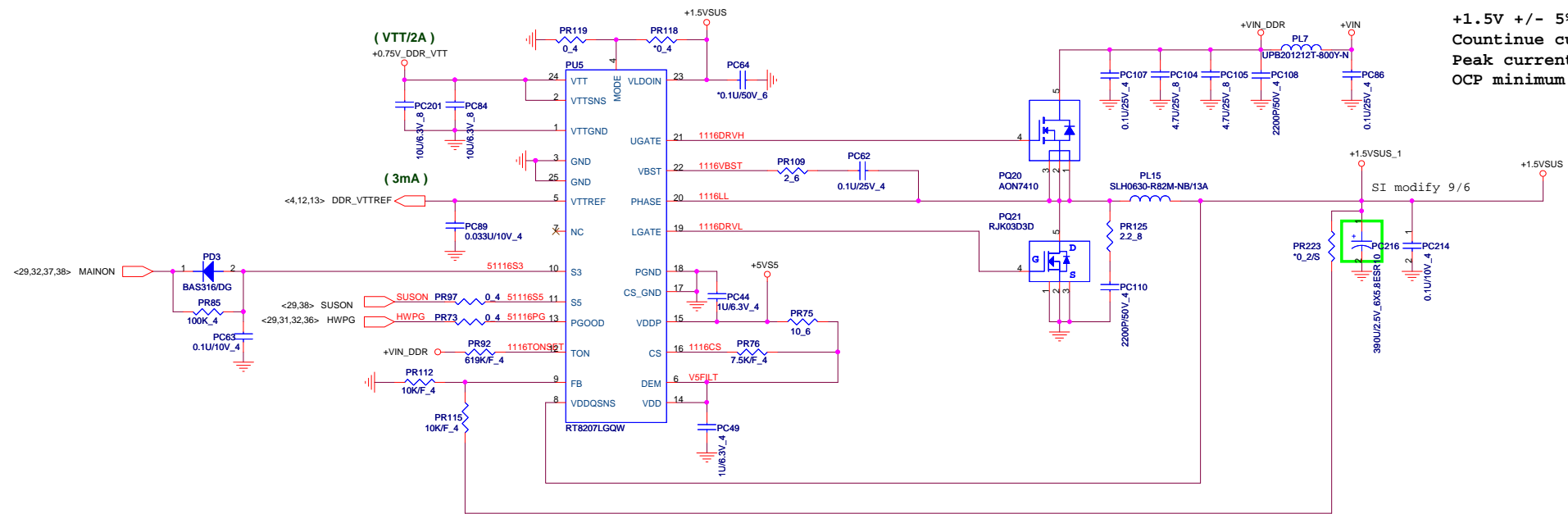
- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils





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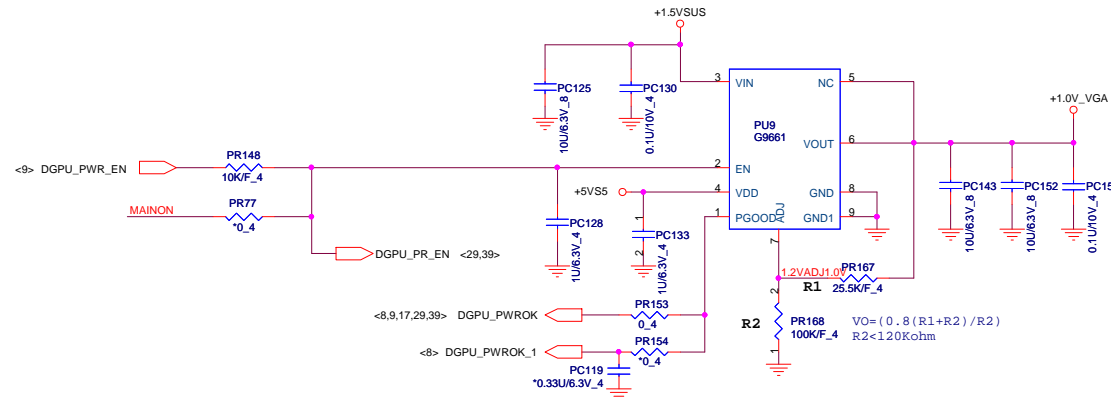




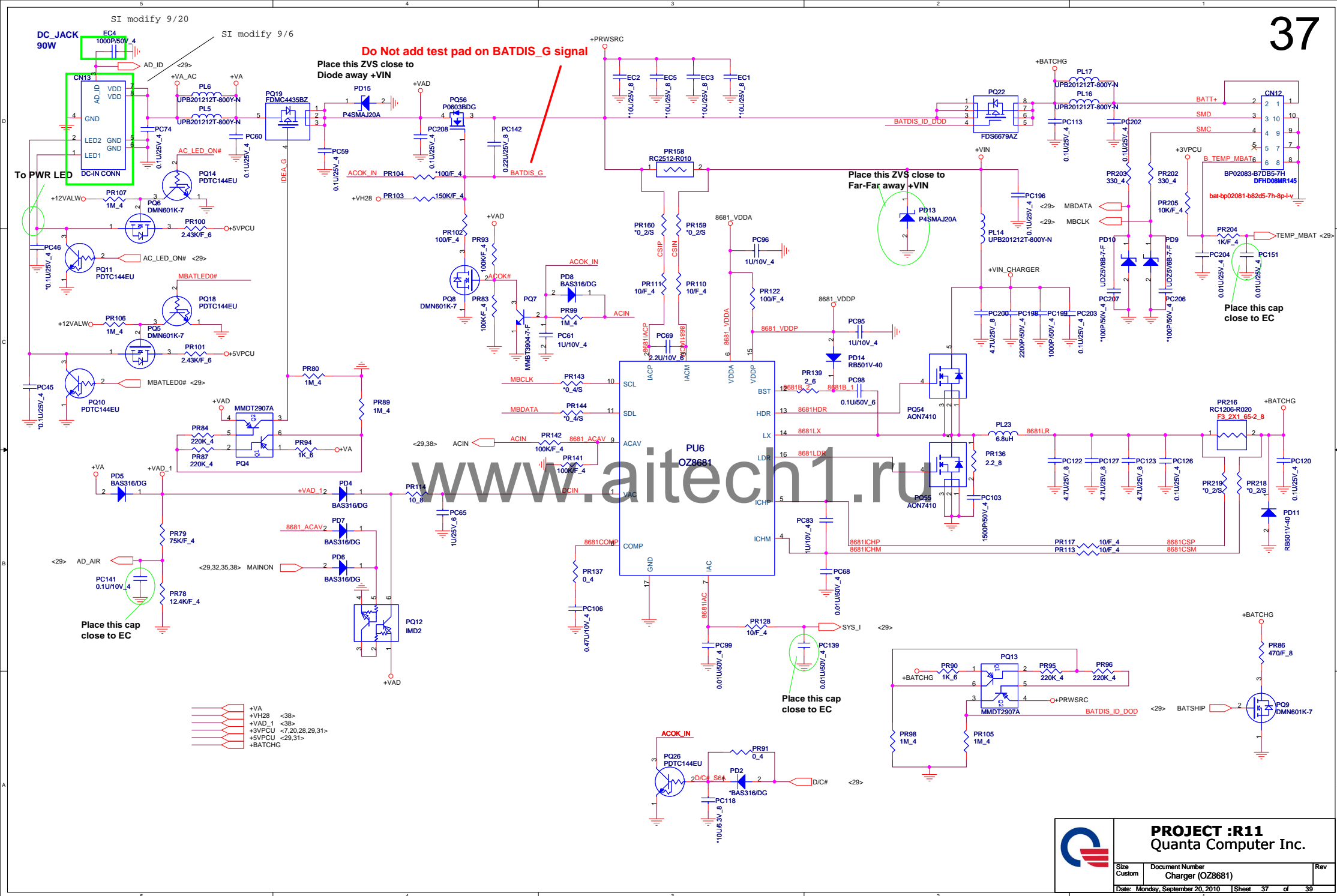
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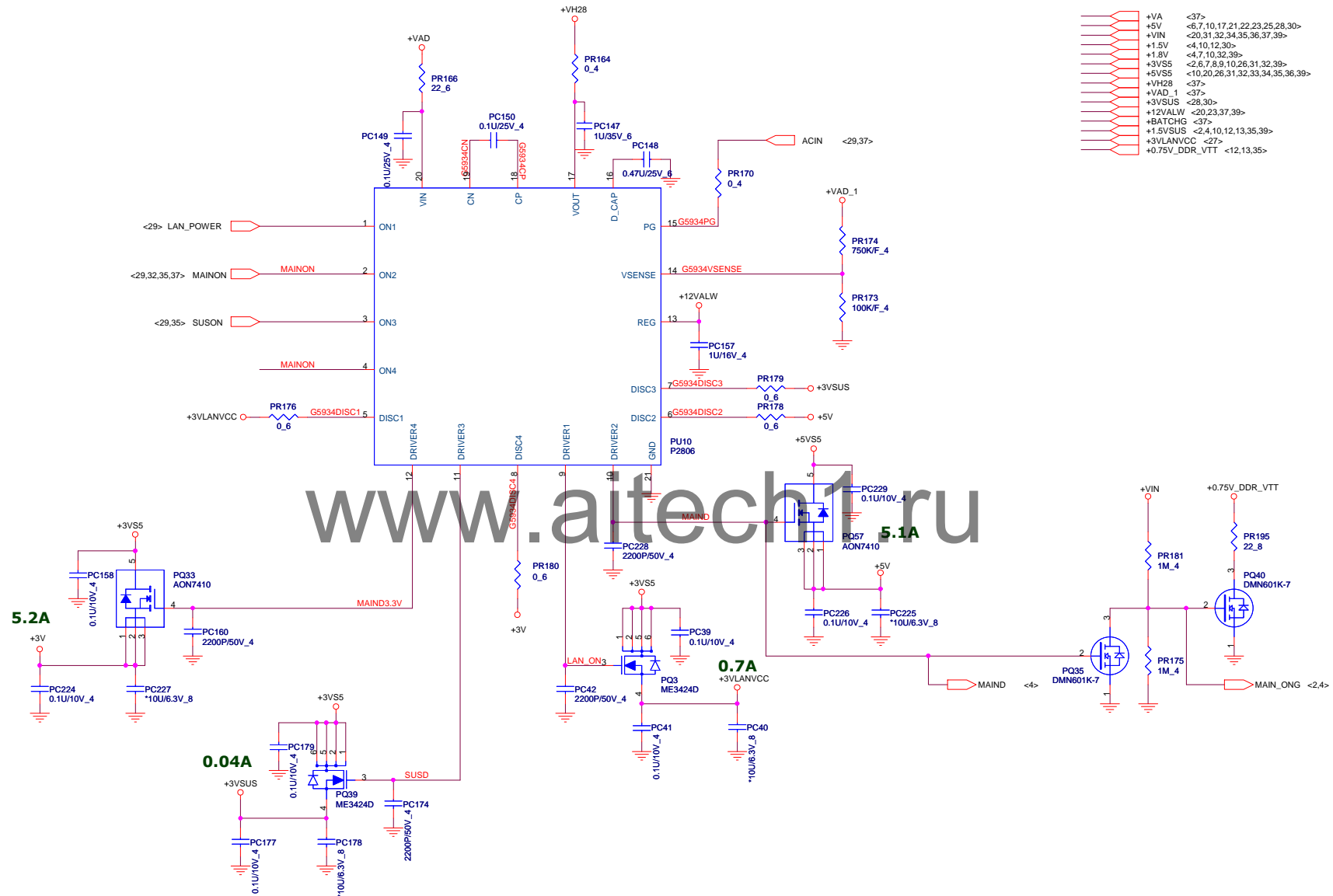
SG & Discrete Only

+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A









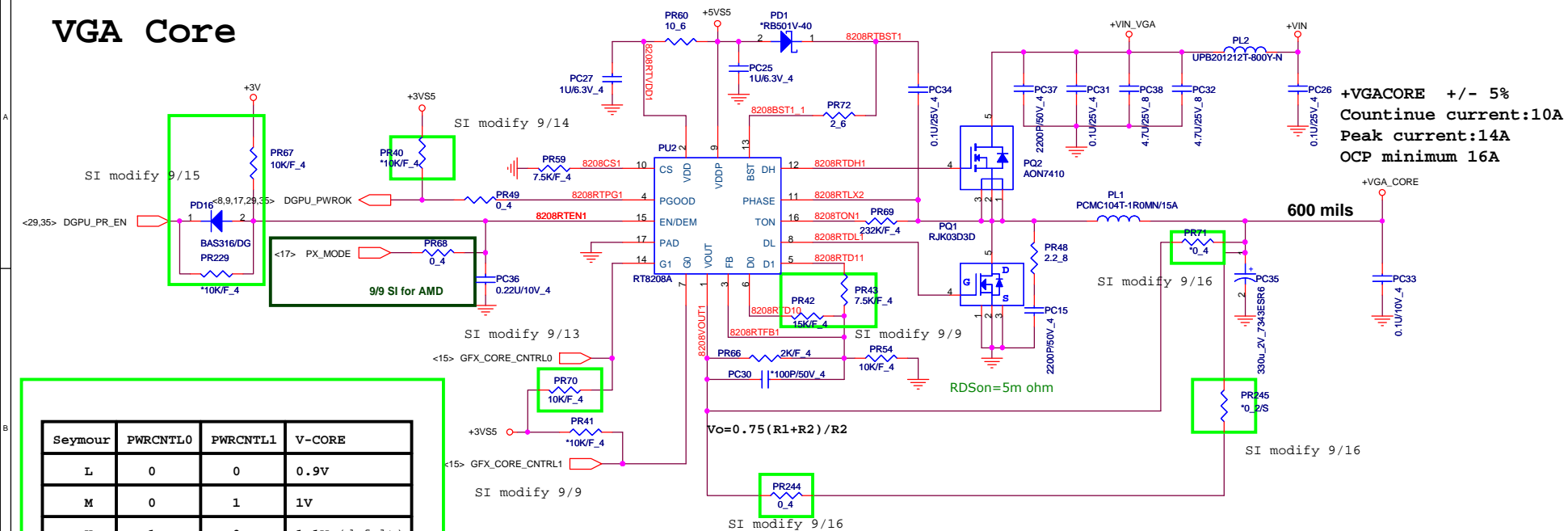
+VA	<37>
+5V	<6,7,10,17,21,22,23,25,28,30>
+VIN	<20,31,32,34,35,36,37,39>
+1.5V	<4,10,12,30>
+1.8V	<4,7,10,32,39>
+3VS5	<2,6,7,8,9,10,26,31,32,39>
+5VS5	<10,20,26,31,32,33,34,35,36,39>
+VH28	<37>
+VAD_1	<37>
+3VSUS	<28,30>
+12VALW	<20,23,37,39>
+BATCHG	<37>
+1.5VSUS	<2,4,10,12,13,35,39>
+3VLANVCC	<27>
+0.75V_DDR_VTT	<12,13,35>



PROJECT :R11
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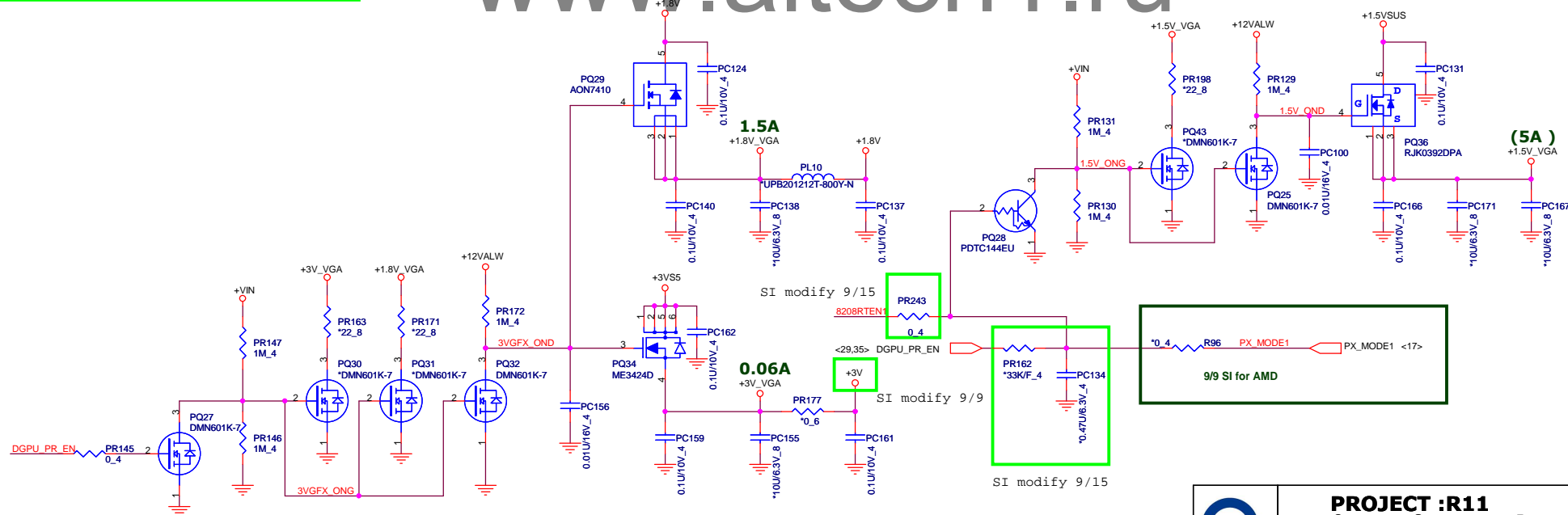
Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	
Date:	Monday, September 20, 2010	Sheet 38 of 39

VGA Core



Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (default)
TBD	1	1	NA

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PROJECT :R11
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Size Custom	Document Number +VGACORE (RT8208/1.8V)	Rev
Date: Monday, September 20, 2010		Sheet 39 of 39